Reduce Energy Losses and THD in Buck Converter Using Control Algorithm

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Abstract—The paper will focus on modeling, analysis, and design and simulation buck converter architecture. This architecture is used for automotive dual power system to reduce filters, dynamic response and power. The converter is designed in CCM (continuous conduction mode). The voltage mode control strategy is proposed by using pulse width modulation (PWM) with a proportional-integral-derivative (PID). The effectiveness of the step down converter is verified through simulation results using control oriented simulator like MATLAB/Simulink tools.

The proposed circuits operate at constant frequency and are regulated by conventional pulse width modulation (PWM) using dedicated PWM and PID control techniques. The circuit operation, mathematical analysis, designs and simulation results for continuous current mode (CCM) operation are mentioned in this paper.

Keywords—Buck Converter, Power factor, Loss, Total Harmonic Distortion, Pulse width modulation and PID control.

I. INTRODUCTION

TABLE I

CLASSIFICATION OF POWER CONVERTER

<table>
<thead>
<tr>
<th>According to output voltage level</th>
<th>• Buck, • Boost, • Buck-Boost</th>
</tr>
</thead>
<tbody>
<tr>
<td>According to mode of energy transfer</td>
<td>• Fly back mode, • Forward mode</td>
</tr>
<tr>
<td>According to control mode</td>
<td>• Voltage mode, • Current mode</td>
</tr>
<tr>
<td>According to Switching method</td>
<td>• ZVS(Zero Voltage Switching), • ZCS(Zero Current Switching)</td>
</tr>
</tbody>
</table>

Basic diagram of Buck converter is shown in fig. 1.

Fig. 1 Basic Block Diagram

Buck converter where L is filter inductor and C is filter capacitor. \( V_0 \) is assumed to remain constant and S is switched at very high frequency. S is ON for time DT and OFF for \((1-D)T\) [2].

Fig. 2 Switch ON and OFF

\( V_L = V_{DC} - V_0 \) for \( 0 < t < DT \) and which is constant also inductor current \( I_L \) increase linearly. And \( V_D = - V_{DC} \) when switch is off, \( V_{DC} = 0 \), so \( V_L = -V_0 \), so \( I_L \) decrease linearly and \( V_S = V_{DC} \) [4]

Consideration of Feedback control to address load regulation of the converter is included. By employing a constant frequency, continuous current Buck converter design with the switching period is defined below in fig. 2. By \( T_2 - T_1 = T \). The converter initially has two conducting states.
defined by periods $T_1 - T_0 = DT$ and $T_2 - T_1 = (1 - D) T$, corresponding to the two switching states. [3]

The $V_{DC}$ supply is connected with the duty cycle $D$, and a complement controlled synchronous switch is applied to complete the connection during the remaining $(1 - D)$ portion of the period. Inductor operating waveform is given below. [6]

\[ \Delta V_c = V_{in} \cdot a \cdot (1 - a) / (8 \cdot L \cdot C \cdot f^2) \]  
\[ \Delta V_{out} = V_{in} \cdot a \cdot (1 - a) / (8 \cdot L \cdot C \cdot f^2) \]

Where, $f=1/T$.

Figure 5 shows the power diagram of power converter using a power MOSFET/IGBT as a switch. As the name implied a step-down (buck) converter produces a lower average output voltage $V_{out}$ than the d.c. input voltage $V_{in}$. By varying the duty-ratio $T_{on}/T$ of the switch, the average output voltage can be controlled. As switch is on at time $t=0$, the supply current which rises flows through the inductor and capacitor and load. Therefore the inductor stores the energy during $T_{on}$ period. During the interval when switch is on, the diode becomes reverse biased and input provides energy to load as well as to the inductor. When switch is off, inductor current flows through L, C, load and freewheeling diode D and hence diode D conducts [7].

Distortion must be considered in any converter or power supply. How much ripple or other unwanted effects will be present at rectifier output? How pure is the output signal of a dc-dc converter or inverter? Regulation defines how closely a power supply output approaches an ideal source. Power factor helps to address system efficiency rather than just converter efficiency. Unity Power Factor (UPF) is an important term in power electronics [10].

When the total power is equal to the real power and thus, the reactive power is zero, unity power factor is achieved. However unity power factor is also affected by the presence of current harmonics. Unity power factor is achieved when only the fundamental current harmonic is present. The benefit of UPF is the converter will appear as a purely resistive load to the power grid. This means the converter will not return any power to the grid or introduce harmonics into the grid. There are also economic benefits to the electricity supplier due to reduced rms currents. Product of the ratio of the primary current harmonic to the total current multiplied by the displacement power factor (DPF). DPF is the same as PF in a linear circuit.[5]

\[ \text{PF} = \frac{i_S}{I_S} \cdot \text{DPF} \]  
\[ i_{S(n)} = I_{S1} + \sum i_{S(n)} \]  

Where,
\[ n=2, 3, 4, 5... \text{ and} \]
\[ i_{S1} \text{ is the fundamental Freq.} \]
Advantages of UPF
- Reduced low frequency voltage and current harmonic to the supply source and regulate DC output voltage.
- High frequency switching harmonics due to chopper may be easily suppressed by the input filter.
- Sensitive to variations of power system impedance.
- Standard regulation can be maintained to meet green power.[8]

A.C. signal is rectified, but before rectification it is pass through EMI filter where the noise or spurious signal is removed and then after it will be passed to the next stage which is power factor correction circuit. The output of the circuit the input power is pulsating (at 100-120 Hz) and, since the power demanded by the load is constant, it is necessary to include an element to store the energy.[11]

III. PROPOSED DESIGN CRITERIA FOR CONVERTER

A. Block diagram

![Fig. 7 Proposed Design](image)

![Fig.8 Design blocks](image)

Steps for design converter:-
- The input AC source is applied to line filter and then through rectifier it is converted into DC. By means of the capacitor this DC is smoothened. [14]
- This DC is applied to the high frequency power conversion stage. The control signal to power conversion stage is provided by the control circuitry.
- Output of high frequency power converter is rectified and filtered to obtain DC output. One of the output voltage sources is used as power source to the control circuit under normal working conditions. [12]
- The control circuit also receives peak current and voltage signal as feedback.

B. Efficiency Improvement criteria.
- Low Rdson for High Duty Cycle
- Schottky Diode
  - Low forward drop
  - Short recovery time
- Inductor
  - Short recovery time Multiple parallel winding such as Bifilar (two windings), Trifilar (three windings)
- Capacitor
  - Low forward drop
  - Short recovery time
  - Paralleling caps (increasing capacitance while reducing ESRs)
- Lower Inductor Ripple
  - Reduce rms loss (inductor and output capacitor)
  - Increase switching frequency or inductance
- Switching loss and real-estate trade off
- Lower gate drive voltage
- Use of Synchronous MOSFET in place of diode, especially for low voltage and high current output
- Replaces freewheeling schottky with MOSFET Especially beneficial on low duty cycle and high current applications
- Due to required dead time and slow MOSFET’s body diode, a Schottky is connected across the synchronous MOSFET[10]

C. Non-ideal buck loss considerations

When efficiency estimation is required in the design, losses in buck circuit should be considered. Several major losses to consider
- Static loss of MOSFET
- Switching loss of MOSFET
- MOSFET gate drive losses
- Static loss of diode
- Switching loss of diode
- Inductor’s copper loss
- Capacitor’s ESR loss[11]

IV. BUCK DESIGN WITH LOSSES

Maximum Output Power (Pomax) = 120W
Nominal Output Voltage (Vonom) = 12V
Nominal Input Voltage(Vinom) = 24V
Switching Frequency (Fs) = 250kHz
Minimum Percent CCM : (Iccm) = 10%
Maximum Ripple % :Vopp = 2%

\[\mu = 1.10^{-6}\]
\[m = 1.10^{-3}\]

Nominal Duty Cycle: D = (Vonom/Vinom)

Critical Inductance: \[Lc = \frac{(Vonom^2}{Iccm \cdot P_{max}} \cdot 2 \cdot Fs}\]

= 12.000H-\mu
Peak Inductor Current: \( I_{lop} = \frac{V_{nom}}{1/(V_{nom}^2/P_{omax}) + (1 - D)/2L_0F_s} \)
\[ = 10.06\text{A} \]

Switch Voltage: \( V_{swmax} = V_{nom} \)
\[ = 24\text{V} \]

Switch Current: \( I_d = D \cdot \frac{P_{omax}}{V_{nom}} \)
\[ = 5\text{A} \]

Choose MOSFET IRF7471 40V 10A \( R_{diode} = 13\text{mOhm} \)

Diode \( V_{rrm} \): \( V_{rrm} = V_{nom} = 24\text{V} \)

Diode Forward Current \( I_d \),
\[ = 5\text{A} \]

Choose MBR3040 schottky diode

Capacitor Voltage Rating:- \( V_{cap} = V_{nom} + \frac{V_{opp}}{2} \)
\[ = 12.12\text{V} \]

Capacitance \( C_0 \),
\[ = \frac{(1-D)}{8L_0F_s} + V_{opp} \]
\[ = 250 \cdot 10^{-3} \]

RMS Current Rating: \( I_{caprms} \),
\[ = \frac{(1-D)}{1.73L_0F_s} V_{nom} \]
\[ = 0.035\text{A} \]

Choose 25V 50 Micro Farad Capacitor.[14]

Due to required dead time and slow MOSFET’s body diode, a Schottky is connected across the Synchronous MOSFET MOSFET+Schottky=FETKY combo such as IRF7326D2 [12].

V. CONTROL TECHNIQUES

The feedback is employed to maintain voltage regulation regardless of disturbances in input voltage, \( v_g(t) \), or load current, \( i_{load}(t) \), or variations in component values. The duty cycle is varied in the feedback loop to compensate for these variations [13].

\[ \text{A voltage reference is used to compare with the output voltage. Sensor gain is used to scale down the output to be equal to voltage reference. The error signal thus generated is fed to the compensator which is the key part to be designed to ensure stability of total feedback loop. Compensator design affects the overshoot, steady state error and transient response of the loop. The PWM block compares the compensator output with another ramp signal to give the variation in duty cycle.} \]

The source from where the ramp signal is generated leads to different control schemes. The three most common control schemes are voltage mode control, current mode control and \( V^2 \) control. Other hybrid schemes are derived from combinations of these control schemes. The effect of feedback loop on the small signal transfer function for all the three control schemes and compensation techniques for each control scheme are discussed.

The GSSA method is presented for modeling the controlled buck converter with a resistive load. The GSSA method is used to derive the dynamic model of the considered system as under[6].

The zero-order approximation with CCM mode. The paper shows how to derive the dynamic model of the system including the PI controllers of the voltage and current loops in which it has not been reported in the previous publications. The intensive time-domain simulations via the software package with the exact topology model are used to validate the proposed model. The results show that a good agreement between both models is achieved. The stability issues are very important. Engineers can use the proposed dynamic model from the paper for the stability analysis to predict the unstable conditions in the future work. In addition, the reported model can drastically reduce the simulation time compared with the exact topology model. Therefore, the reported model is suitable for the controller designs by using the control system techniques to achieve the best system performance [7].

VI. DESIGN AND SIMULATION RESULTS

In the figure given below, the voltage range for output is 12V and input voltage is given as 24V. So range of the input voltage is 22V to 26V DC. Here the transfer Function is calculated by using KCL and KVL for buck converter. The simulation is performed on MATLAB/SIMULINK.

Here, the response of the system is checked without feedback (open loop) and with feedback (closed loop) system using PID control which is shown in the following figures.
VII. CONCLUSION

In the available techniques, initial flow of current is very high. In the field of control engineering, maximum 10% overshoot is acceptable. The value of peak overshoot current is 12.8 amp. In the proposed techniques, reduce the peak overshoot up to 8.1 amp as shown in the fig. 18 and 19. In the proposed techniques, total harmonics 23% reduced compare to available techniques.

The suggested techniques improve the energy loss at startup and sudden changes in the load. So here, regulation is improved.

REFERENCES