

understanding of the capabilities and limitations of specialized high temperature electronic systems allows a third option, which is a craft that maintains high level, complex, low power electronics within the protective environmental enclosure, while allowing select subsystems to operate within the ambient environment of the planet. This option, as illustrated in Fig. 2, minimizes the cost and thermal load required to maintain a large volume of instrumentation at a significantly lower temperature than the ambient environment, while limiting the cost of high temperature electronic development efforts to critical subsystems that do not require complex circuitry.

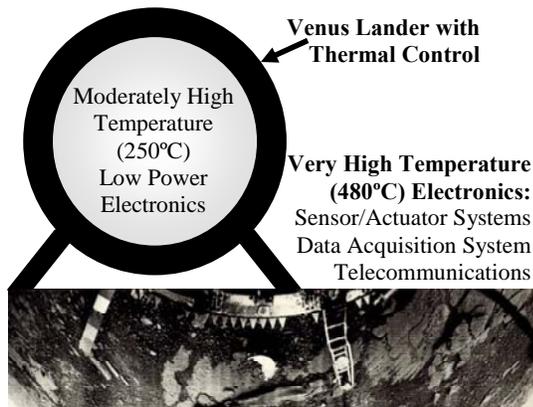


Fig. 2. Schematic of hybrid Venus Lander concept.

As illustrated in Fig. 2, there are several critical electronic subsystems, including sensor/ actuator systems, data acquisition systems and telecommunications. Regarding sensor, actuator and data acquisition subsystems, the goal is to maintain the required signal conditioning, signal amplification and control electronics close to the sensors and actuators with which they are associated. This reduces thermal leakage through the cabling port on the Lander as well as increasing the signal to noise ratio for the sensors. Much of the remaining electronics and instruments will need to be protected from the harsh Venus surface environment via a pressure vessel that is thermally controlled using either insulation alone or a combination of active cooling and insulation. Since maintaining heat generating electronic systems within the vessel greatly increases the amount of power required to maintain the desired internal temperature and reduces overall mission lifetime, the development of 500°C electronics will allow the removal of high heat dissipating subsystems, such as signal transmitters for telecom, power converters, and actuator drive electronics from the pressure vessel.

As described for the Venus lander, the majority of the electronics required for a Mars rover would be held within the warm electronics box (WEB) that maintains the electronics within the military specified range of temperatures. Currently, sensor, actuator and data acquisition subsystems are kept within the WEB and are connected with their associated sensors through a complex network of heavy cables that run throughout the rover. Maintaining the required signal conditioning, signal amplification and control electronics close to the sensors and actuators with which they are associated would significantly reduce the weight and complexity of the system, while increasing the signal to noise ratio for the sensors.

2. ELECTRONIC PACKAGING

Electronic Packaging includes all of the passive components and materials used to connect integrated circuits (or individual devices) and sensors to each other and with the outside world. As shown in the Fig. 3 schematic, First-level packaging includes the signals directly connected to the device (within a package) and Second-level packaging includes the packaged active and passive devices as well as the printed circuit board that connects them. This paper will focus on the extreme environment challenges associated with First and Second Level Packaging.

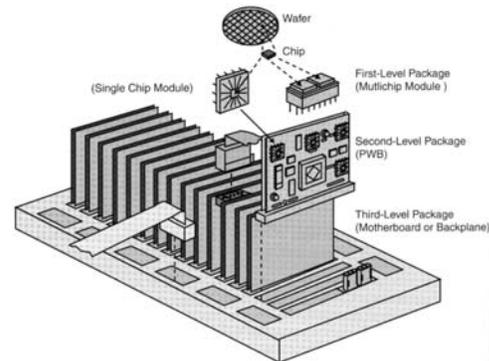


Fig. 3. Schematic illustrating the three levels of electronic packaging.[1]

Failure of electronic packaging for extreme environments can be separated into two different categories, over-stress and time-dependent failure mechanisms, as detailed in Fig. 4. Over-stress mechanisms are those that occur immediately upon exposure to the target environment and test conditions. Examples include plastic deformation, melting of materials, and change in resistance or capacitance with increasing temperature. Conversely, time dependent degradation of

electronic packages relate to processes that occur over many cycles or after extended exposure to the target operating conditions. Examples include fatigue, creep, diffusion, oxidation, changes in resistance or capacitance with time at temperature, and electromigration. The dominant failure mechanism for packages exposed to the Mars ambient environment is fatigue, which is influenced by phase transformations, embrittlement at these low temperatures, and especially the coefficient of thermal expansion (CTE) mismatch between the different materials. Due to the high temperatures of the Venus ambient environment, failure mechanisms of serious concern for electronic packages include material degradation, plastic deformation, creep, diffusion, oxidation, and electromigration.

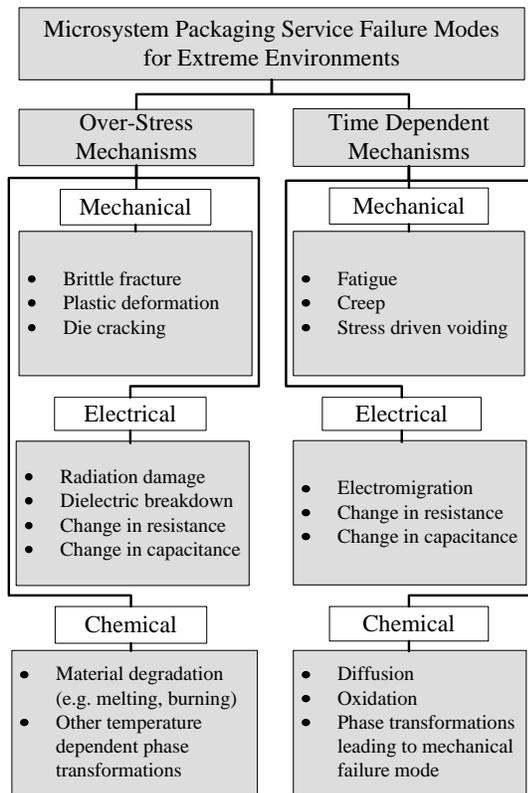


Fig. 4. Illustration describing failure mechanisms for electronic packages exposed to extreme environments.

3. MARS

Failure of electronic packages exposed to the low temperature thermal cycles of Mars is dominated by fatigue, which is the phenomenon of material failure under cyclic loading conditions. For electronic packaging, fatigue generally results from large temperature fluctuations and CTE differences between adjoining materials. As shown in Fig. 5,

examples of sites at which fatigue becomes a problem are solder joints, die attachment points, and wirebonds. The room temperature fatigue life of gold as a function of stress amplitude is shown in Fig. 6. For electronic packages exposed to the Mars ambient thermal cycles, the fatigue life of the gold wirebonds is influenced by global and local thermal expansion mismatches between: (i) glob-top encapsulant and the silicon die, (ii) encapsulant and the wire, and (iii) encapsulant and the substrate assembly. For a wirebond chip-on-board assembly with a rigid encapsulant, the region above the ball bond has been found to be the predominant failure site.[2] This finding agrees well with the failed wirebond shown in Fig. 7, which was located on a chip on board assembly that was encapsulated with a rigid epoxy and thermal cycled from -125 to $+85^{\circ}\text{C}$ (a relevant Mars ambient condition).

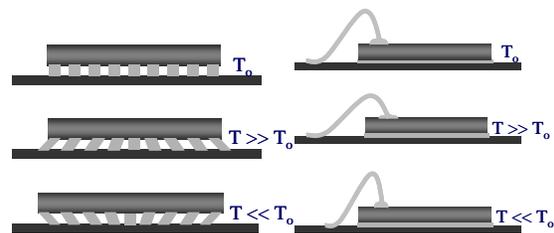


Fig. 5. Schematic illustrating the influence of temperature for materials with differing CTEs.

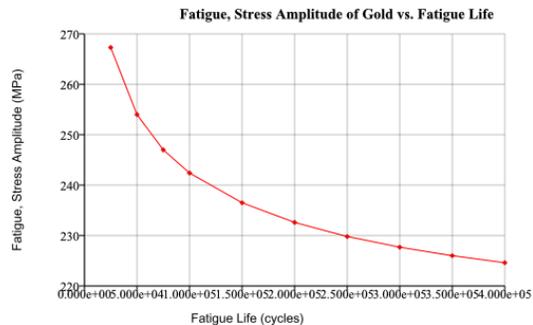


Fig. 6. Plot of room temperature fatigue strength as a function of cycles for gold.[3]

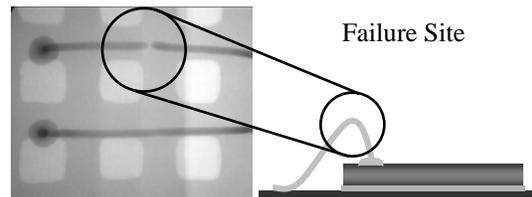


Fig. 7. An X-ray image of a failed wirebond and a schematic illustrating the location of failure.

Phase transformations that influence fatigue resistance, mechanical behaviour and electrical behaviour can also occur at the low temperatures of the Mars thermal cycle. Of particular concern are

the glass transition temperatures of the polymers used in the assemblies. This temperature can result in significant changes in the elastic moduli and CTEs of polymers.

4. VENUS

Due to the high temperatures of the Venus ambient environment, issues such as the degradation of materials with temperature, interdiffusion of metal layers, and oxidation become significant. Although the minimal thermal cycles experienced within the dense atmosphere of the Venus surface eliminates the issue of fatigue discussed previously, the CTE differences between the die and the substrate combined with the significant temperature differential observed during the single thermal cycle result in a sustained stress at the elevated temperature, which in turn causes problems such as high temperature tensile failure and creep. In addition, phase and microstructural changes combined with diffusion and oxidation influence the strength, ductility and conductivity of the different materials. Finally, all of these issues combined with the applied current can yield electromigration problems. The correct selection of materials for electronic packaging within the Venus environment can help minimize several of these issues, while in other cases trade-offs must be made between several competing mechanisms in order to promote the survival of the overall subsystem.

4.1 Melting and Degradation of Materials

Traditional microelectronic packaging relies heavily on the use of polymers for applications such as printed wiring boards, die attach and conformal coating. Since all of the traditional polymers used in electronic packaging degrade (melt or burn) below Venus surface temperatures, alternate materials and configurations must be used. In addition, various passivation materials used for thin film circuits may melt or soften, exposing the highly reactive materials underneath, as shown in Fig. 8 below.

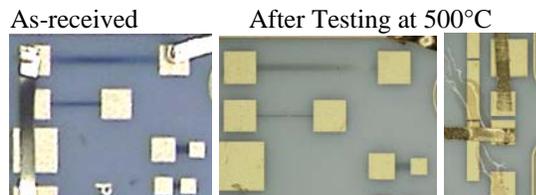


Fig. 8. Optical photograph of thin film resistors, before and after long term testing at 500°C.

With respect to die attach materials, which are used to attach the backside of a chip to the substrate that connects the device to other passive and active devices, most of those used for commercial applications on Earth melt at significantly lower temperatures than those required for Venus. A set of solder and braze considered for this application are summarized in Table 1, along with their melting temperatures. One of the techniques used to minimize temperature excursions during processing is to use lower melting temperature solders than the required application and rely on diffusion to modify the composition of the attach material. This will be discussed further in the following section.

Table 1. Maximum use temperatures for various die attach materials.

	Max. Temp. (°C)	Comments
Solders		
Au80Sn20	280	Eutectic
Au88Ge12	356	Eutectic
Au97Si3	363	Eutectic
Sn5Pb95	308	Solidus
Pb92In5Ag3	300	Solidus
Brazes		
82Au/18In	451	Solidus
45Ag/38Au/17Ge	525	Eutectic
72Ag/28Cu	780	Eutectic
82Au/18Ni	950	Eutectic
Other		
Au thick film paste	> 600	High firing temperature
Au thermo-compression bonding	> 800	Assumes Au to Au interface

4.2 Diffusion, Solid State Phase Transformation and Oxidation

Diffusion, the net transport of matter to minimize a concentration gradient or a free energy gradient, is significantly dependent upon temperature and time. This phenomenon is illustrated schematically in Fig. 9, which shows two different metals, Au and Ni, in intimate contact with each other, along with the associated concentration of Au, before and after extended exposure at an elevated temperature.[4] As mentioned in the previous section, this can be used advantageously for die attach materials as a means of modifying the composition of the alloy to that of one that is more amenable to the application. This process can be better described in relation to the phase diagram shown in Fig. 10. If Au-Sn solder of concentration C1 is placed in direct contact with pure Au, the composition of the alloy can change to C2 following extended exposure at elevated temperature. The amount of time required

for this concentration change is dependent upon the temperature of exposure and the respective diffusivities of Au and Sn.

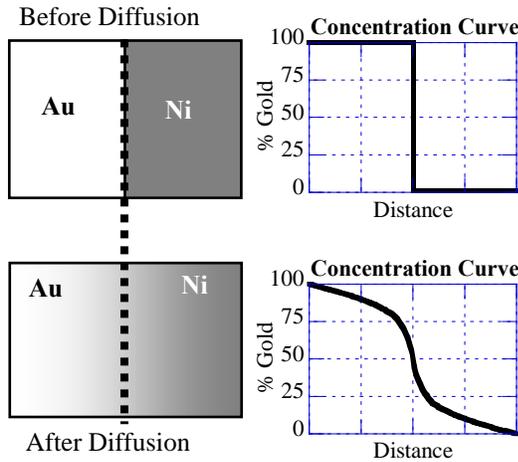


Fig. 9. Schematic illustrating interdiffusion of metals for Au-Ni diffusion couple.

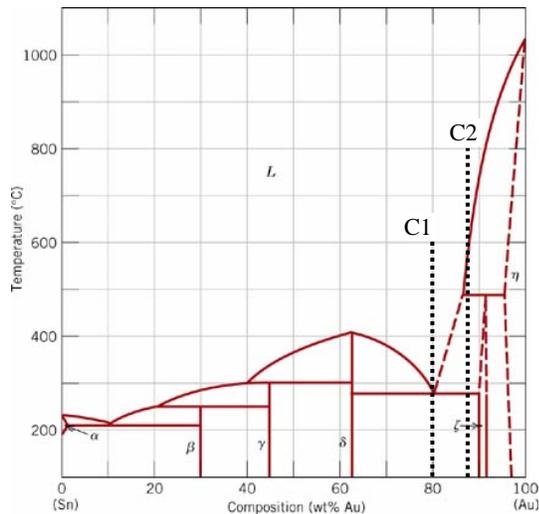


Fig. 10. Au-Sn binary phase diagram. [5]

Since there tend to be several different metal layers on both the die and the substrate, one must be careful to avoid the selection of attachment materials that will yield weak or brittle intermetallic phases following the solid state phase transformations that often accompany the interdiffusion of multiple metals. Fig. 11 exhibits the formation of secondary phases following the exposure of an assembly with a SiC device attached to a Cu-Ni-Au plated substrate using a Au-Ge die attach material to 500°C. Composition of the resulting brittle Ge-Ni intermetallic phase is shown in Fig. 12.

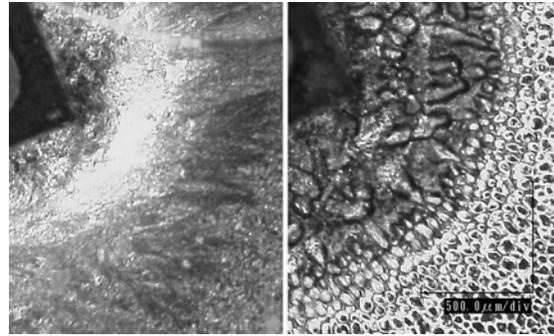


Fig. 11. Optical photograph of die attach material, before (left) and after (right) exposure at 500°C.

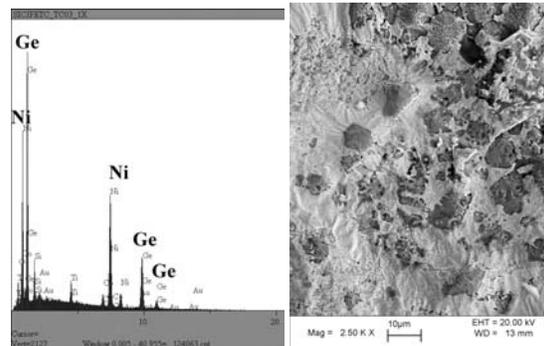


Fig. 12. EDS and SEM micrograph of GeNi phase.

The most dangerous diffusion-related failure mechanism for Venus electronics is the oxidation of metal to semiconductor contacts on the SiC devices. The diffusion of O₂ through the outer metal layers to the base metal forming the metal to semiconductor contact results in the oxidation of this base metal and a subsequent increase in the contact resistance. Development and implementation of diffusion barrier layers capable of minimizing oxidation along with device design optimization to minimize the effect contact resistance on circuit functionality are both required.

4.3 Elevated Temperature Deformation

Due to the many interfaces present within electronic assemblies, the stresses observed are closely related to the CTE, strength, and elastic modulus for each of the materials involved, along with environmental parameters, such as temperature excursions, and design parameters, such as die size. A plot of CTEs as a function of temperature for various materials used in high temperature assembly is provided in Fig. 13. Stress distributions between adjoining materials can be minimized by selecting materials with CTEs that are more closely matched over the entire range of exposure temperatures.

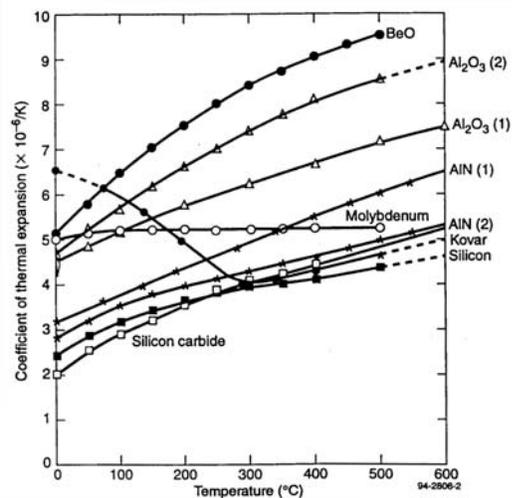


Fig. 13. Coefficients of thermal expansion as a function of temperature for various materials used in high temperature electronic assemblies. [6]

If the CTEs of the device and the substrate are not exactly matched, the stresses at the interface will steadily increase from a minimum at the center of the device to a maximum at its edges. As shown in Fig. 14, which summarizes the strength of various Pb-Sn solder alloys as a function of temperature, strength tends to reduce as temperature increases. In this application, this situation is exacerbated by the fact that the stresses within the die attach increase as a function of temperature as well. If the die attach is too weak it may fail following initial exposure.

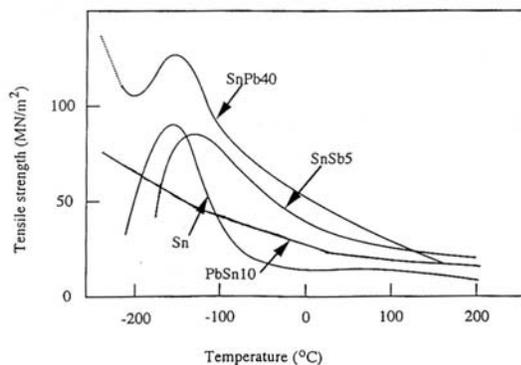


Fig. 14. Tensile strength as a function of temperature for various Pb-Sn solders. [6]

Assuming that the stresses are below the yield strength of the material, time and temperature dependent deformation, or creep, may still occur. Since creep is both time and temperature dependent, creep may occur at temperatures as low as 0.3 times the melting temperature (T_m) of the material; however, appreciable creep deformation within a reasonable amount of time is expected at

temperatures above $0.5T_m$. The influence of temperature and applied stress on creep strain and time to failure is illustrated in Fig. 15. Creep of Au, which has a melting temperature of 1337K (1064°C), will become a significant concern above about 668K (395°C).

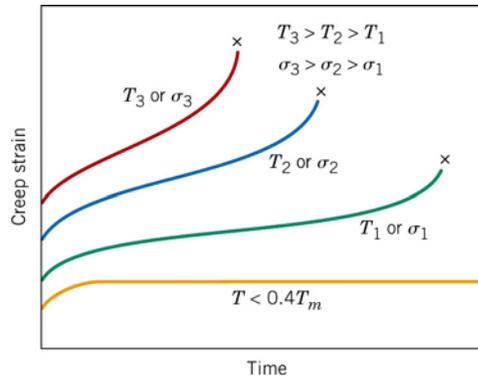


Fig. 15. Schematic illustrating the influence of temperature and stress on creep strain and time to failure. [4]

4.4 Electromigration

Due to the role of diffusion in electromigration and the fact that most active devices capable of working at elevated temperatures are power devices, electromigration becomes a considerable concern for high temperature electronic systems. Factors influencing electromigration include: current density, temperature, grain structure, temperature gradients, passivation coating selection (adhesion/degradation), surface structure and migration, stress distribution within the metal film, distribution and selection of metal layers, alloying effects, surface roughness, and CTE mismatch among the different layers. A schematic illustrating the influence of temperature and current density on electromigration is shown in Fig. 16.

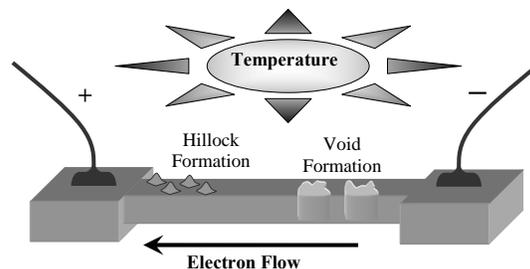


Fig. 16. Schematic illustrating the influence of temperature and current density on electromigration.

