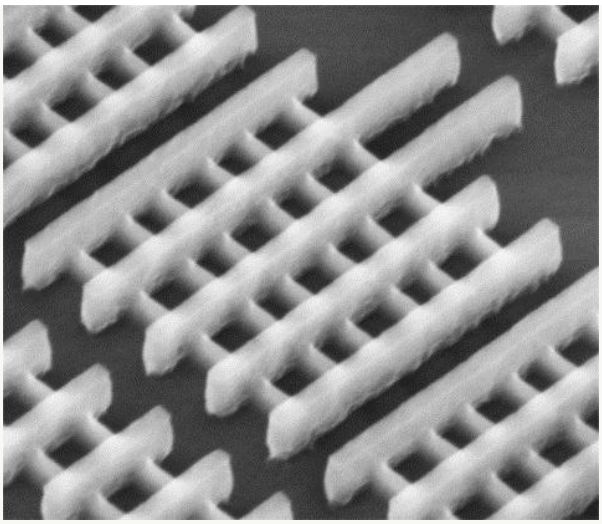
THE AIR IS GETTING THINNER FOR SILICON'S COMPETITORS



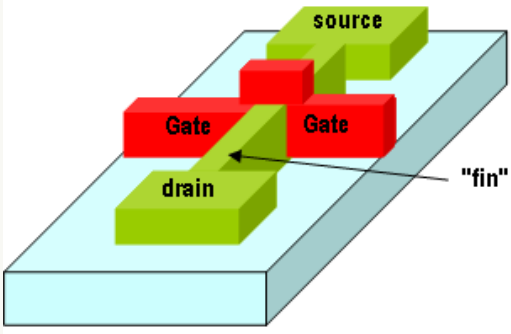
Intel's 3D tri-gate transistors have a feature size of only 22 nm. The thin structures are the silicon channels, the thicker ones are the gates and the contacts. Several gates can be used next to each other to enhance the efficiency of the switching. (c) Intel

Finally I am getting around to blog about the latest generation of transistors that Intel presented earlier this months. These transistors reach feature sizes of only 22 nanometres, down from 32 nm. To give you some perspective what this amazingly high integration means: 4,000 of those 22 nm structures fit across the *width* of a human hair, or similarly, 100 million of these transistors fit on the head of a pin.

Now how did they reduce transistor length scales down by almost a third? Well, even though Intel (and others) is in the business of shrinking transistor for more

than 40 years, this time it's a bit more than a mere scaling exercise. For the first time we have a commercial 3D transistor design on such a scale. In a typical 'field-effect' transistor, two electrical contacts are used to run an electric current through a silicon layer. The transistor is switched between an electrically conducting and an insulating state by a gate on top of the silicon. The voltage applied to that gate determines whether current can flow or not. Thereby the gate is able to set the digital '1' and '0' in a transistor.

A problem in shrinking transistors has been the fact that those three electric contacts need a certain minimum space of their own. Furthermore, as the gate has become smaller and smaller, it has been increasingly inefficient to switch the electric current in the silicon layer underneath. For smaller gates the electric fields from the gate just don't reach that far down into the silicon layer.



The 3D transistor fin architecture. Image by Irene Ringworm via wikimedia.

In the new design, which isn't only pursued by Intel but also by others, engineers now have left the flat architecture and do what architects in cities around the world

have done to make use of limited real state: go vertical. As you can see from the image on the right, now the gate doesn't only contact from the top, but wraps around a thin 'fin' of silicon.

This design has several advantages. It not only takes up less space, but contacting the silicon channel from three sides also means that the transistors are faster to switch. The Intel transistors can be switched up to a hundred billion times a second. And finally, the electrical fields from the gate have a more immediate effect on the current through the fin. That means that the voltage that needs to be applied to the gate is much lower, which saves up to 50% in active power.

The technology roadmap suggests a further reduction in size to 14 nm by 2013, and to 10 nm by 2015(!). And looking at the fin structures, it seems possibly to squeeze them further together, provided that the lithography processes used to make such structures can keep up.

So, the big question is how are the alternatives to silicon transistors in light of this tough competition?

Well, there is a 2007 *Nature* paper by James Heath and colleagues from Caltech, that reports a device with a 10^{11} bits per square centimetre storage density based on crossing nanowires. These nanowires are 16 nm wide, and 33 nm spaced apart.

That means storage densities seem still higher than the latest silicon transistors, but on the other hand this is unproven technology with quite a few errors across the chip, and limited life times.

And as for graphene? Looking on some of the fastest graphene devices made so far, well these have channel lengths of 140 nm, although I am sure this can be further reduced. The bond length between carbon atoms is 0.14 nanometers, so graphene could be scaled to similar sizes as those transistors. The only problem is that the edges of graphene at these length scales could mean a far more erratic behaviour in transistor operation, so I'd be hesitant to see the big potential yet.

Indeed, it seems that none of these technologies offers a compelling alternative to silicon so far. Of course, silicon has all the advantages of an entrenched technology. You can beat silicon only if you're considerably ahead of the trend for silicon transistors, and offer a more cost-efficient solution. But seeing this latest progress in 3D transistor designs, the air is certainly getting thinner for the contenders for silicon's crown. Perhaps it will still be possible to improve on silicon in terms of speed and power consumption, but it seems unlikely it will happen on size.

Source: http://allthatmatters.heber.org/2011/05/26/the-air-is-getting-thinner-for-silicons-competitors/