The Common Emitter Amplifier Circuit

In the Bipolar Transistor tutorial, we saw that the most common circuit configuration for an NPN transistor is that of the Common Emitter Amplifier circuit and that a family of curves known commonly as the Output Characteristic Curves, relate the transistors Collector current ($I_c$), to the output or Collector voltage ($V_{ce}$), for different values of Base current ($I_b$).

All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value so some way of "presetting" the amplifier circuit to operate between these two maximum or peak values is required. This is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

We also saw that a static or DC load line can be drawn onto these output characteristics curves to show all the possible operating points of the transistor from fully "ON" to fully "OFF", and to which the quiescent operating point or Q-point of the amplifier can be found. The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).

To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement. The best possible position for this Q-point is as close to the centre position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, ie. $V_{ce} = 1/2V_{cc}$. Consider the Common Emitter Amplifier circuit shown below.
The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing". This type of biasing arrangement uses two resistors as a potential divider network across the supply with their center point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits. This method of biasing the transistor greatly reduces the effects of varying Beta, \( \beta \) by holding the Base bias at a constant steady voltage level allowing for best stability. The quiescent Base voltage \( V_b \) is determined by the potential divider network formed by the two resistors, \( R_1, R_2 \) and the power supply voltage \( V_{cc} \) as shown with the current flowing through both resistors.

Then the total resistance \( R_T \) will be equal to \( R_1 + R_2 \) giving the current as \( i = \frac{V_{cc}}{R_T} \). The voltage level generated at the junction of resistors \( R_1 \) and \( R_2 \) holds the Base voltage \( V_b \) constant at a value below the supply voltage. Then the potential divider network used in the common emitter amplifier circuit divides the input signal in proportion to the resistance. This bias reference voltage can be easily calculated using the simple voltage divider formula below:

\[
V_B = \frac{V_{cc} \cdot R_2}{R_1 + R_2}
\]

The same supply voltage, \( V_{cc} \) also determines the maximum Collector current, \( I_C \) when the transistor is switched fully "ON" (saturation), \( V_{ce} = 0 \). The Base current \( I_B \) for the transistor is found from the Collector current, \( I_C \) and the DC current gain Beta, \( \beta \) of the transistor.

\[
\beta = \frac{\Delta I_C}{\Delta I_B}
\]

Beta is sometimes referred to as \( h_{FE} \) which is the transistors forward current gain in the common emitter configuration. Beta has no units as it is a fixed ratio of the two currents, \( I_C \) and \( I_B \) so a small change in the Base current will cause a large change in the Collector current. One final point about Beta. Transistors of the same type and part number will have large variations in their Beta value for example, the BC107 NPN Bipolar transistor has a DC current gain Beta value of between 110 and 450 (data sheet value) this is because Beta is a characteristic of their construction and not their operation.

As the Base/Emitter junction is forward-biased, the Emitter voltage, \( V_e \) will be one junction voltage drop different to the Base voltage. If the voltage across the Emitter resistor is known then the Emitter current, \( I_e \) can be easily calculated using Ohm's Law. The Collector current, \( I_C \) can be approximated, since it is almost the same value as the Emitter current.

**Example No1**
A common emitter amplifier circuit has a load resistance, $R_L$ of $1.2\,\text{k}\Omega$ and a supply voltage of $12\,\text{V}$. Calculate the maximum Collector current ($I_C$) flowing through the load resistor when the transistor is switched fully "ON" (saturation), assume $V_{CE} = 0$. Also find the value of the Emitter resistor, $R_E$ with a voltage drop of $1\,\text{V}$ across it. Calculate the values of all the other circuit resistors assuming an NPN silicon transistor.

$$I_{C_{(\text{MAX})}} = \frac{V_{CC} - V_{RE}}{R_L} = \frac{12 - 1}{1200} = 9.2\,\text{mA}$$

$$V_{CE} = 0 \text{ (Saturation)}$$

This then establishes point "A" on the Collector current vertical axis of the characteristics curves and occurs when $V_{CE} = 0$. When the transistor is switched fully "OFF", there is no voltage drop across either resistor $R_E$ or $R_L$ as no current is flowing through them. Then the voltage drop across the transistor, $V_{CE}$ is equal to the supply voltage, $V_{CC}$. This then establishes point "B" on the horizontal axis of the characteristics curves. Generally, the quiescent Q-point of the amplifier is with zero input signal applied to the Base, so the Collector sits half-way along the load line between zero volts and the supply voltage, $(V_{CC}/2)$. Therefore, the Collector current at the Q-point of the amplifier will be given as:

$$I_{C_{(Q)}} = \frac{12-1}{1200} = \frac{5.5}{1200} = 4.58\,\text{mA}$$

This static DC load line produces a straight line equation whose slope is given as: $-1/(R_L + R_E)$ and that it crosses the vertical $I_C$ axis at a point equal to $V_{CC}/(R_L + R_E)$. The actual position of the Q-point on the DC load line is determined by the mean value of $I_B$.

As the Collector current, $I_C$ of the transistor is also equal to the DC gain of the transistor (Beta), times the Base current ($\beta \times I_B$), if we assume a Beta ($\beta$) value for the transistor of say 100, (one hundred is a reasonable average value for low power signal transistors) the Base current $I_B$ flowing into the transistor will be given as:

$$\beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{4.58\,\text{mA}}{100} = 45.8\,\mu\text{A}$$

Instead of using a separate Base bias supply, it is usual to provide the Base Bias Voltage from the main supply rail ($V_{CC}$) through a dropping resistor, $R_1$. Resistors, $R_1$ and $R_2$ can now be
chosen to give a suitable quiescent Base current of 45.8μA or 46μA rounded off. The current flowing through the potential divider circuit has to be large compared to the actual Base current, \( I_B \), so that the voltage divider network is not loaded by the Base current flow. A general rule of thumb is a value of at least 10 times \( I_B \) flowing through the resistor \( R_2 \). Transistor Base/Emitter voltage, \( V_{be} \) is fixed at 0.7V (silicon transistor) then this gives the value of \( R_2 \) as:

\[
R_2 = \frac{V_{RE} + V_{BE}}{10 \times I_B} = \frac{1 + 0.7}{458 \times 10^{-6}} = 3.71k\Omega
\]

If the current flowing through resistor \( R_2 \) is 10 times the value of the Base current, then the current flowing through resistor \( R_1 \) in the divider network must be 11 times the value of the Base current. The voltage across resistor \( R_1 \) is equal to \( V_{cc} - 1.7v \ (V_{RE} + 0.7 \text{ for silicon transistor}) \) which is equal to 10.3V, therefore \( R_1 \) can be calculated as:

\[
R_1 = \frac{V_{cc} \cdot (V_{RE} + V_{BE})}{11 \times I_E} = \frac{12 - 1.7}{504 \times 10^{-6}} = 20.45k\Omega
\]

The value of the Emitter resistor, \( R_E \) can be easily calculated using Ohm's Law. The current flowing through \( R_E \) is a combination of the Base current, \( I_B \) and the Collector current \( I_C \) and is given as:

\[
I_E = I_C + I_B = 4.58mA + 45.8\mu A = 4.63mA
\]

Resistor, \( R_E \) is connected between the Emitter and ground and we said previously that it has a voltage of 1 volt across it. Then the value of \( R_E \) is given as:

\[
R_E = \frac{V_{RE}}{I_E} = \frac{1v}{4.63mA} = 216\Omega
\]

So, for our example above, the preferred values of the resistors chosen to give a tolerance of 5% (E24) are:

\[
R_1 = 20k\Omega, \ R_2 = 3.6k\Omega, \ R_L = 1.2k\Omega, \ R_E = 220\Omega
\]

Then, our original Common Emitter Amplifier circuit above can be rewritten to include the values of the components that we have just calculated above.

**Completed Common Emitter Circuit**
**Coupling Capacitors**

In Common Emitter Amplifier circuits, capacitors $C_1$ and $C_2$ are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not effected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, $C_E$ is included in the Emitter leg circuit.

This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only $R_L$ plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, $C_E$ is chosen to provide a reactance of at most, $1/10$th the value of $R_E$ at the lowest operating signal frequency.

**Output Characteristics Curves**

Ok, so far so good. We can now construct a series of curves that show the Collector current, $I_C$ against the Collector/Emitter voltage, $V_{CE}$ with different values of Base current, $I_B$ for our simple common emitter amplifier circuit. These curves are known as the "Output Characteristic Curves" and are used to show how the transistor will operate over its dynamic range. A static or DC load line is drawn onto the curves for the load resistor $R_L$ of $1.2k\Omega$ to show all the transistors possible operating points.

When the transistor is switched "OFF", $V_{CE}$ equals the supply voltage $V_{CC}$ and this is point $B$ on the line. Likewise when the transistor is fully "ON" and saturated the Collector current is determined by the load resistor, $R_L$ and this is point $A$ on the line. We calculated before from the DC gain of the transistor that the Base current required for the mean position of the transistor was $45.8\mu A$ and this is marked as point $Q$ on the load line which represents the Quiescent state.
point or Q-point of the amplifier. We could quite easily make life easy for ourselves and round off this value to 50μA exactly, without any effect to the operating point.

**Output Characteristics Curves**

Point Q on the load line gives us the Base current Q-point of $I_B = 45.8μA$ or $46μA$. We need to find the maximum and minimum peak swings of Base current that will result in a proportional change to the Collector current, $I_C$ without any distortion to the output signal. As the load line cuts through the different Base current values on the DC characteristics curves we can find the peak swings of Base current that are equally spaced along the load line. These values are marked as points N and M on the line, giving a minimum and a maximum Base current of 20μA and 80μA respectively.

These points, N and M can be anywhere along the load line that we choose as long as they are equally spaced from Q. This then gives us a theoretical maximum input signal to the Base.
terminal of 60μA peak-to-peak, (30μA peak) without producing any distortion to the output signal. Any input signal giving a Base current greater than this value will drive the transistor to go beyond point N and into its Cut-off region or beyond point M and into its Saturation region thereby resulting in distortion to the output signal in the form of "clipping".

Using points N and M as an example, the instantaneous values of Collector current and corresponding values of Collector-emitter voltage can be projected from the load line. It can be seen that the Collector-emitter voltage is in anti-phase (-180°) with the collector current. As the Base current Ib changes in a positive direction from 50μA to 80μA, the Collector-emitter voltage, which is also the output voltage decreases from its steady state value of 5.8v to 2.0v.

Then a single stage Common Emitter Amplifier is also an "Inverting Amplifier" as an increase in Base voltage causes a decrease in Vout and a decrease in Base voltage produces an increase in Vout. In other words the output signal is 180° out-of-phase with the input signal.

**Voltage Gain**

The **Voltage Gain** of the common emitter amplifier is equal to the ratio of the change in the input voltage to the change in the amplifiers output voltage. Then \( \Delta V_L \) is \( V_{out} \) and \( \Delta V_B \) is \( V_{in} \). But voltage gain is also equal to the ratio of the signal resistance in the Collector to the signal resistance in the Emitter and is given as:

\[
\text{Voltage Gain} = \frac{V_{out}}{V_{in}} = \frac{\Delta V_L}{\Delta V_E} = -\frac{R_L}{R_E}
\]

We mentioned earlier that as the signal frequency increases the bypass capacitor, \( C_E \) starts to short out the Emitter resistor. Then at high frequencies \( R_E = 0 \), making the gain infinite. However, bipolar transistors have a small internal resistance built into their Emitter region called \( R_e \). The transistors semiconductor material offers an internal resistance to the flow of current through it and is generally represented by a small resistor symbol shown inside the main transistor symbol.

Transistor data sheets tell us that for a small signal bipolar transistors this internal resistance is the product of \( 25mV \div I_e \) (25mV being the internal volt drop across the Base/Emitter junction depletion layer), then for our common Emitter amplifier circuit above this resistance value will be equal to:

\[
R_e = \frac{25mV}{I_E} = \frac{25mV}{4.58mA} = 5.5\Omega
\]

This internal Emitter leg resistance will be in series with the external Emitter resistor, \( R_E \), then the equation for the transistors actual gain will be modified to include this internal resistance and is given as:
At low frequency signals the total resistance in the Emitter leg is equal to $R_E + R_e$. At high frequency, the bypass capacitor shorts out the Emitter resistor leaving only the internal resistance $R_e$ in the Emitter leg resulting in a high gain. Then for our common emitter amplifier circuit above, the gain of the circuit at both low and high signal frequencies is given as:

**At Low Frequencies**

$$\text{Gain} = -\frac{R_L}{(R_E + R_e)} = -\frac{1200}{220 + 5.5} = -5.32$$

**At High Frequencies**

$$\text{Gain} = -\frac{R_L}{R_e} = -\frac{1200}{5.5} = -218$$

One final point, the voltage gain is dependent only on the values of the Collector resistor, $R_L$ and the Emitter resistance, $(R_E + R_e)$ it is not affected by the current gain Beta, $\beta$ ($h_{FE}$) of the transistor.

So, for our simple example above we can now summarise all the values we have calculated for our common emitter amplifier circuit and these are:

<table>
<thead>
<tr>
<th></th>
<th>Minimum</th>
<th>Mean</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Current</td>
<td>20μA</td>
<td>50μA</td>
<td>80μA</td>
</tr>
<tr>
<td>Collector Current</td>
<td>2.0mA</td>
<td>4.8mA</td>
<td>7.7mA</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>2.0V</td>
<td>5.8V</td>
<td>9.3V</td>
</tr>
<tr>
<td>Amplifier Gain</td>
<td>-5.32</td>
<td>-218</td>
<td>-218</td>
</tr>
</tbody>
</table>

**Common Emitter Amplifier Summary**

Then to summarize. The **Common Emitter Amplifier** circuit has a resistor in its Collector circuit. The current flowing through this resistor produces the voltage output of the amplifier. The value of this resistor is chosen so that at the amplifiers quiescent operating point, **Q-point** this output voltage lies half way along the transistors load line.

The Base of the transistor used in a common emitter amplifier is biased using two resistors as a potential divider network. This type of biasing arrangement is commonly used in the design of bipolar transistor amplifier circuits and greatly reduces the effects of varying Beta, ( $\beta$ ) by holding the Base bias at a constant steady voltage. This type of biasing produces the greatest stability.
A resistor can be included in the emitter leg in which case the voltage gain becomes \(-\frac{R_L}{R_E}\). If there is no external Emitter resistance, the voltage gain of the amplifier is not infinite as there is a very small internal resistance, \(R_e\) in the Emitter leg. The value of this internal resistance is equal to 25mV/I_E

Source:

http://www.electronics-tutorials.ws/amplifier/amp_2.html