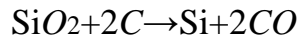


Silicon Growth

How is it possible for the IC industry to continue to make such gains, and how do they build so many circuits on one chip anyway? In order for us to be able to understand this, we have to take a look at the **monolithic fabrication process**. *Lith* comes from the Greek word for stone, and *mono* means one, of course. Thus, monolithic construction refers to building the circuit in "one stone" or in one single crystal substrate.

In order for us to do this however, we first of all need the "stone", so let's see where that comes from.

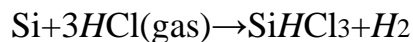
We start out with a natural form of silicon which is very abundant (and relatively pure); quartzite or SiO_2 (sand). In fact, silicon is one of the most abundant elements on the earth. This is reacted in a furnace with carbon (from coke and/or coal) to make what is known as **metallurgical grade silicon** (MGS) which is about 98% pure, via the reaction



(1)

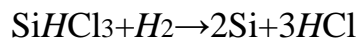
We have seen that on the order of 10^{14} impurities will make major changes in the electrical behavior of a piece of silicon. Since there are about 5×10^{22} atoms/cm³ in a silicon crystal, this means we need a purity of better than 1 part in 10^8 or 99.999999% pure material. Thus we have a long way to go from the purity of the MGS if we want to make electronic devices that we can use in silicon.

The silicon is crushed and reacted with HCl (gas) to make trichlorosilane, a high vapor pressure liquid that boils at 32°C as in:



(2)

Many of the impurities in the silicon (aluminum, iron, phosphorus, chromium, manganese, titanium, vanadium and carbon) also react with the HCl , forming various chlorides. One of the nice things about the halogens is that they will react with almost anything. Each of these chlorides have different boiling points, and so, by fractional distillation, it is possible to separate out the SiHCl_3 from most of the impurities. The (pure) trichlorosilane is then reacted with hydrogen gas (again at an elevated temperature) to form pure **electronic grade silicon** (EGS).



(3)

Although the EGS is relatively pure, it is in a polycrystalline form which is not suitable for device manufacture. The next step in the process is to grow single crystal silicon which is usually done via the **Czochralski** (pronounced "chaw-krawl-ski") method to make what is sometimes called CZ silicon. The Czochralski process involves melting the EGS in

a crucible, and then inserting a seed crystal on a rod called a puller which is then slowly removed from the melt. If the temperature gradient of the melt is adjusted so that the melting/freezing temperature is just at the seed-melt interface, a continuous single crystal rod of silicon, called a **boule**, will grow as the puller is withdrawn.

Figure 1 is a diagram of how the Czochralski process works. The entire apparatus must be enclosed in an argon atmosphere to prevent oxygen from getting into the silicon. The rod and the crucible are rotated in opposite directions to minimize the effects of convection in the melt. The pull-rate, the rotation rate and the temperature gradient must all be carefully optimized for a particular wafer diameter and growth direction. The $\langle 111 \rangle$ direction (along a diagonal of the cubic lattice structure) is usually chosen for wafers to be used for bipolar devices, while the $\langle 100 \rangle$ direction (along one of the sides of the cube) is favored for MOS applications. Currently, wafers are typically 6" or 8" in diameter, although 12" diameter wafers (300 mm) are looming on the horizon.

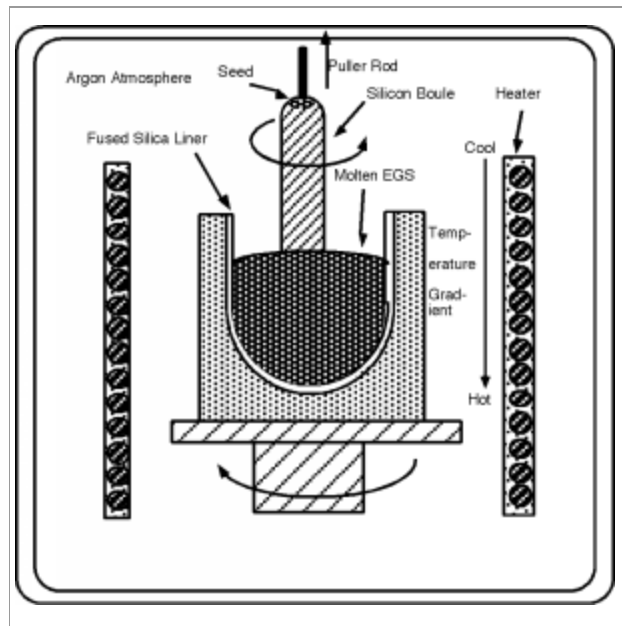


Figure 1: Czochralski crystal growth

Once the boule is grown, it is ground down to a standard diameter (so the wafers can be used in automatic processing machines) and sliced into wafers, much like a salami. The wafers are etched and polished, and move on to the process line. A point to note however, is that due to "kerf" losses (the width of the saw blade) as well as polishing losses, more than half of the carefully grown, very pure, single crystal silicon is thrown away before the circuit fabrication process even begins!

Source: <http://cnx.org/content/m1033/latest/?collection=col10114/latest>