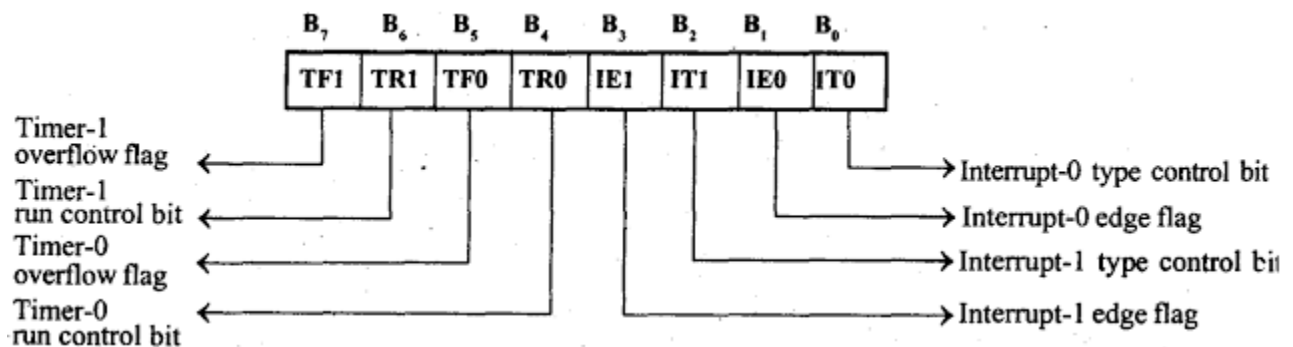


REGISTERS OF 8051/8031 MICROCONTROLLER

Timer Control Register (TCON):

- The TCON register consists of timer overflow flags, timer run control bits, external interrupt flags and external interrupt type control bits.
- The format of TCON register is,



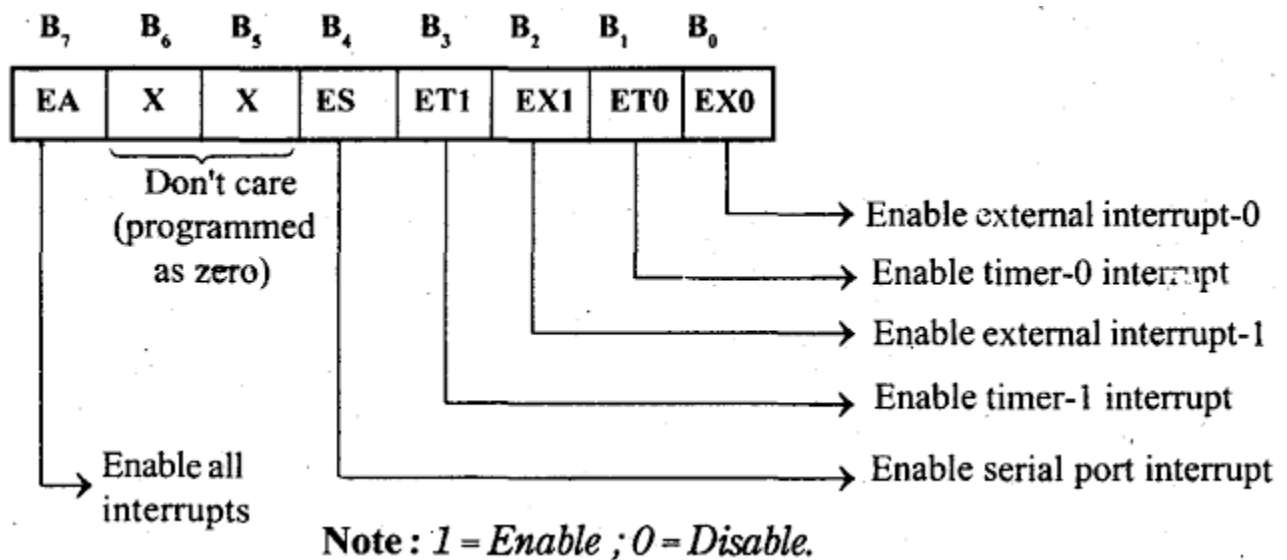
- When clock signal is applied, after reaching maximum value (i.e., the content of counter is all 1's), the content of counter will become zero (i.e., all 0s). This condition is called timer overflow and this is also the end of timing maintain by using the timer.
- The TCON register has a 1-bit flag, TF for each timer to indicate the timer overflow or end of timing.
- Whenever the timer/counter overflows, the TF flag is set to one.
- The TF flag is also used as an interrupt signal to initiate the execution of a subroutine. When the controller executes a subroutine, the TF flag is cleared.
- The TR bit is used to start/stop the timer/counter. When TR bit is set to one, the timer/ counter will start counting and continue the counting as long as TR bit is one. The timer/counter will stop

counting when TR bit is cleared to zero.

- When a valid external interrupt signal is detected the IE flag is set to one. When the controller accepts the external interrupt and start processing it, the IE flag is cleared to zero.
- The IT = 1, when it recognize falling edge triggered external interrupt and IT = 0, when it recognize logic low level external interrupt.

Interrupt Enable Register (IE):

- The IE register is used to enable/disable the interrupts of 8051.
- The interrupts are recognized by the controller only if they are enabled.
- The format of IE register is,



- If EA = 0, then it disable all the five interrupts of 8051.
- If EA = 1, then it enable the interrupts. The EA bit is also called global enable.

Interrupt Priority Register (IP):

- The 8051 has five interrupts.
- The normal priority of these interrupts from highest to lowest are external interrupt-0, Timer-0 interrupt, External interrupt- 1, Timer-1 interrupt and serial Port interrupt.
- The IP register can be programmed to make the priority of any of the interrupt as highest.
- When the priority bit of a particular bit is programmed as one then its priority will be highest.
- The format of IP register is,

