PHASE LOCKED LOOP

Basic Block Diagram of a PLL

Forward path

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        Phase              Low Pass          Voltage
 f_IN   Detector           Filter            Controlled      f_OUT
                                             Oscillator
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f_{IN}

Input

frequency

Feedback path
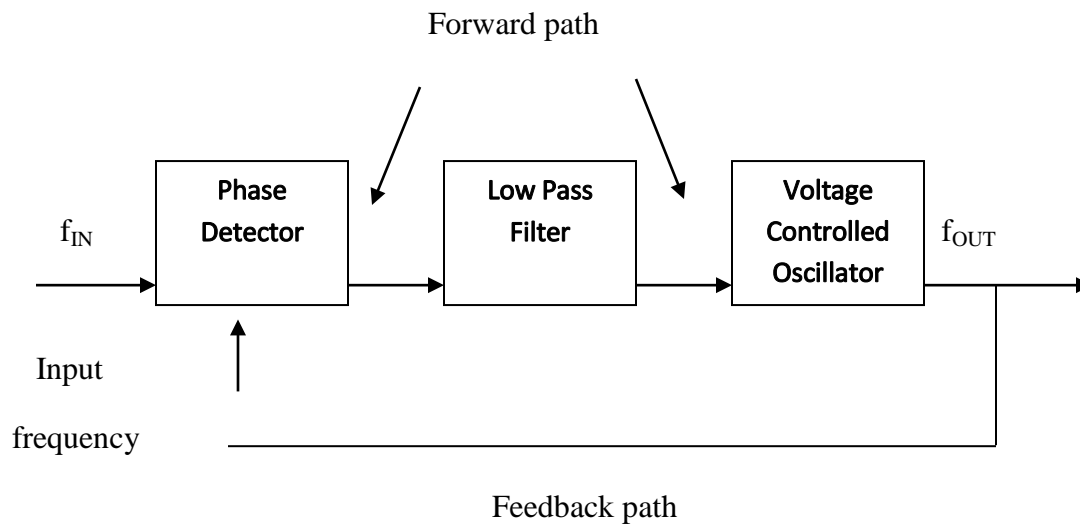
phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency f_{OUT}.

- The output of the phase detector is proportional to the phase difference between f_{IN} & f_{OUT}. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.

- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.

- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.

- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action. If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_o)$ is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference φ. This phase difference φ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

(a) Phase Detector:

Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer

Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

Ex-OR Phase Detector:

This uses an exclusive OR gate. The output of the Ex-OR gate is high only when f_{IN} or f_{OUT} is high.

The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians or 180 degrees. The slope of the curve between 0 or Π radians is the conversion gain k_p of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain K_p is

$$K_P = \frac{5V}{P} = 1.59V / RAD$$

Edge Triggered Phase Detector:

Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e, the output of the detector changes its logic state on the positive edge of the inputs f_{IN} & f_{OUT}

Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.
  R✷ Reference

  V✷ Variable or 0feedback input

  PU ✷ Pump Up signal

  PD✷Pump Down signal

  UF ✷ Up frequency output signal

  DF ✷ Down frequency output signal

(b) Low – Pass filter:

        The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

- Lock range(Tracking range):

  The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency f_{IN}.

- Capture range:

  Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

- Filter Bandwidth:

  Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

(c) Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.

f_{IN} → | Voltage Controlled Oscillator | → $_{UT}$

Input

frequency