NEW DEVICES-FINFET AND SOI MOSFET

Scaling of conventional MOSFET devices deeper into the nanometer side are threatened by the short channel effects. Hence new devices are under research and development stage that can overcome short channel effects. FinFET and FD SOI MOSFET are such new semiconductor devices that promise the possibility of further scaling of the device. Both devices overcome the problem of short channel effects and parasitic capacitance effects.

FinFET

General MOSFET at submicron level is suffering from several submicron issues like short channel effects, threshold voltage variation etc. FinFET is proposed to overcome the short channel effects. Structure of FinFET is shown in Figure (1).

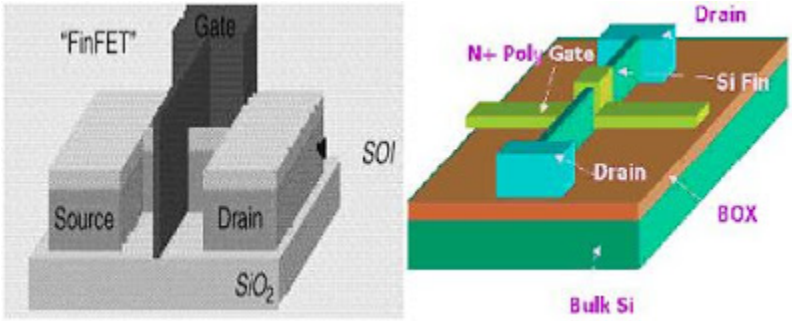

Figure (1) Structure of FinFET [2] [3]

Silicon on insulator (SOI) process is used to fabricate FinFET. This process ensures the ultra thin specifications of device regions. In FinFET electrical potential throughout the channel is controlled by the gate voltage. This is possible due to the proximity of gate control electrode to the current conduction path between source and drain. These characteristics of the FinFET minimize the short channel effect.

Advantages of the FinFET over its bulk-si counterpart are as follows:

1. Conventional MOSFET manufacturing processes can also be used to fabricate FinFET.
2. FinFET provides better area efficiency compared to MOSFET.
3. mobiblity of the carriers can be improved by using FinFET process in conjunction with the strained silicon process.

FinFET device structure

Silicon on Insulator (SOI) process is used to manufacture FinFET. A single poly silicon layer is deposited over a fin. Thus poly silicon straddles the fin structure to form perfectly aligned gates. Here fin itself acts as a channel and it terminates on both sides of source and drain. In general MOSFET device, over the Si substrate poly silicon gate is formed. Poly silicon gate controls the channel. Straddling of poly silicon gate over the Si fin gives efficient gate controlled characteristics compared to MOSFET.

Since gate straddles the fin the length of the channel is same as that of width of the fin. As there are two gates effectively around the fin we can write, width of the channel is equivalent to twice the height of the fin i.e. w=2*h.

A term called “fin pitch” is used to define the space between two fins. Height of the FinFET is equivalent to width of the MOSFET. If w is the fin pitch then to attain same area efficiency required fin height is w/2. But practical experiments have shown that fin height can be greater than w/2 for a fin pitch of w. thus FinFET achieves more area efficiency than MOSFET.

FinFET process technology

SOI technology is used for the fabrication of FinFET. In SOI technology, an insulator, SiO2, isolates the bulk from the substrate. An extremely shallow junction is formed due to the depth limitation put by the insulator. The dielectric isolation and elimination of latch up problem are the advantages of the SOI process.

The FinFET fabrication process steps are showed in the Figure (2). On a thin SOI layer Si3N4 and SiO2 are deposited. Electron beam lithography is used to form silicon fin. Channel length and channel width are determined by the accuracy of the fin. Poly silicon with pentavalent impurities and then oxide layer is deposited over the silicon fin. Then source and drain regions are separated and insulator spacers are formed. Then the etching process is carried out on spacer till silicon fin is reached. Gate is formed by depositing the gate layer.

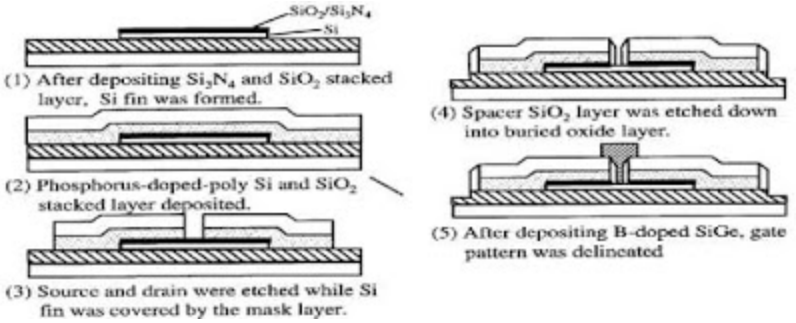

Figure (2) FinFET process flow steps [2]

Silicidation is performed to decrease the high source drain resistance which is formed due to very thin layers of source and drain.

Fully Depleted SOI MOSFET

Structure of FD SOI MOSFET is as shown in the Figure (3).

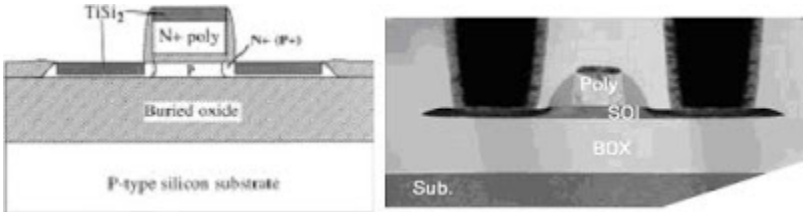

Figure (3) Cross section of an n (p)-channel thin-film SOI MOSFET [1]

Fabrication Process

FD SOI MOSFET is fabricated using a standard fully-depleted SOI CMOS process with N+ polysilicon gate. P-type SIMOX substrates having a resistivity of 20 are used as starting material. Oxidation and oxide strip reduces film thickness to 100 nm. Then LOCOS process is carried out. To adjust the threshold voltages a 30 nm thick gate oxide is grown and boron is implanted. Polysilicon is then deposited and N type is doped. To form source and drain arsenic is implanted. Then oxide deposition and reactive ion etching form 150 nm thick spacer. Then silicidation process is carried out. In this process 30 nm thick titanium layer is deposited and annealed. This process reduces sheet resistance. A nitride or oxide layer is deposited contact holes are opened to access the device. Formation of a passivation layer completes the process.

Advantages of FD SOI MOSFET over bulk CMOS MOSFET

Advantages of FD SOI MOSFET over bulk MOSFET is as follows:

1. Reduced parasitic capacitances and leakage current are achieved due to dielectric isolation.

2. Sharper sub threshold slope, lower body effect and smaller vertical field mobility degradation are achieved with full depletion operation of thin film SOI MOSFETs.

3. Drive capability is increased for low voltage designs.

4. SOI CMOS process for FD SOI MOSFET is simpler compared to its counterpart. This results in minimized threshold voltage roll off, reliable ultra shallow junctions, complete elimination of latch up problem.

Source : http://asic-soc.blogspot.in/2008/01/new-devices-finfet-and-soi-mosfet.html