LOW POWER DESIGN TECHNIQUES

Michael Keating et al. [1] lists several low power techniques to tackle the dynamic and static power consumption in modern SoC designs. Dynamic power control techniques include clock gating, multi voltage, variable frequency, and efficient circuits. Leakage power control techniques include power gating, multi Vt cells. Common methods supported by EDA tools include clock gating, gate sizing, low power placement, register clustering, low power CTS, multi Vt optimization.

Some of the low power techniques in use today are listed in below table.

Traditional Techniques	Dynamic power reduction	Leakage power reduction	Other power reduction techniques
--Clock gating --Power gating --Variable frequency --Variable voltage supply --Variable device threshold	--Clock gating --Power efficient circuits --Variable frequency --Variable voltage supply --Voltage Islands	--Minimize usage of low Vt cells --Power gating --Back biasing --Reduce oxide thickness --Use FinFET	--Multi oxide devices --Minimize capacitance by custom design --Power efficient circuits

Different Low Power Techniques [3]

Power-reduction Technique	Power Benefit	Timing Penalty	Area Penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Multi-Vt Optimization	Medium	Little	Little	Low	Low	None	Low
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi-supply Voltage	Large	Some	Little	High	Medium	Low	Medium
Power Shut-off	HUGE	Some	Some	High	High	High	High
Dynamic and Adaptive Voltage Frequency Scaling	Large	Some	Some	High	High	High	High
Substrate Biasing	Large	Some	Some	Medium	None	None	High

Trade-offs associated with the various power management techniques [2]

Above table summarizes trade-offs associated with different power management techniques. Power gating and DVFS demand large methodology change whereas multi vt and clock gating affect least. Unless large leakage optimization is not necessary it is always beneficial to go with either multi vt or clock gating techniques. Based on the design complexity and requirements combination of any low power techniques can be adopted. Multi vt optimization along with the power gating is found to be efficient in some of the complex designs. Advanced improvements in the implementation (i.e. fabrication) technology has allowed substrate biasing techniques to be used heavily as it does not pose any architectural and design verification challenges and also provides high leakage reduction.

Source : http://asic-soc.blogspot.in/2008/04/low-power-design-techniques.html