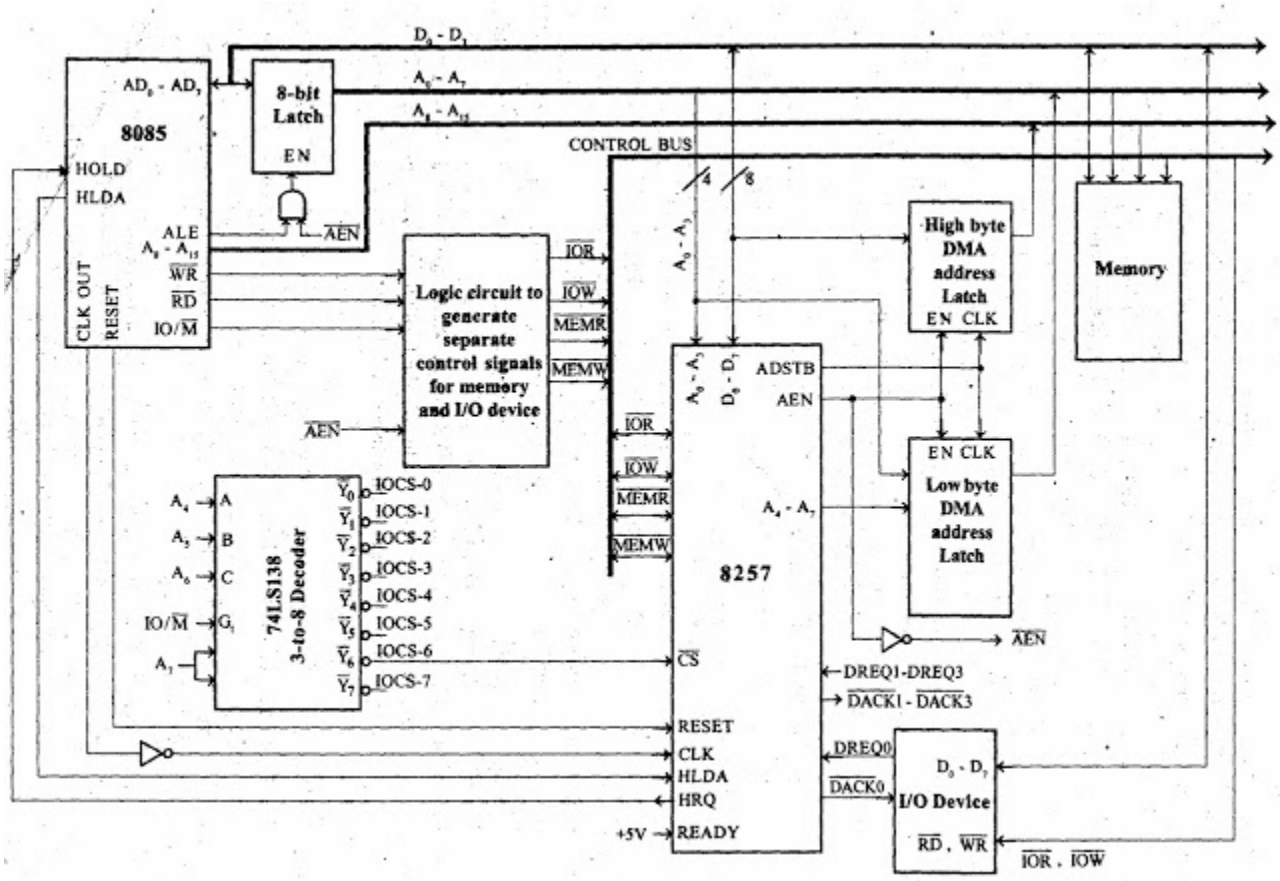
INTERFACING OF 8257 WITH 8085 PROCESSOR

- A simple schematic for interfacing the 8257 with 8085 processor is shown.
- The 8257 can be either memory mapped or I/O mapped in the system.
- In the schematic shown in figure is I/O mapped in the system.
- Using a 3-to-8 decoder generates the chip select signals for I/O mapped devices.
- The address lines A4, A5 and A6 are decoded to generate eight chip select signals (IOCS-0 to IOCS-7) and in this the chip select signal IOCS-6 is used to select 8257.
- The address line A7 and the control signal IO/M (low) are used as enable for decoder.



- The D0-D7 lines of 8257 are connected to data bus lines D0-D7 for data transfer with processor during programming mode.

- These lines (D0-D7) are also used by 8257 to supply the memory address A8-A15 during the DMA mode.

- The 8257 also supply two control signals ADSTB and AEN to latch the address supplied by it during DMA mode on external latches.

- Two 8-bit latches are provided to hold the 16-bit memory address during DMA mode. During DMA mode, the AEN signal is also used to disable the buffers and latches used for address, data and control signals of the processor.

- The 8257 provide separate read and write control signals for memory and I/O devices during DMA.

- Therefore the RD (low), WR (low) and IO/M (low) of the 8085 processor are decoded by a suitable logic circuit to generate separate read and write control signals f memory and I/O devices.

- The output clock of 8085 processor should be inverted and supplied to 8257 clock input for proper operation.

- The HRQ output of 8257 is connected to HOLD input of 8085 in order to make a HOLD request to the processor.

- The HLDA output of 8085 is connected to HLDA input of 8257, in order to receive the acknowledge signal from the processor once the HOLD request is accepted.

- The RESET OUT of 8085 processor is connected to RESET of 8257.

- The I/O addresses of the internal registers of 8257 are listed in table.

Register	Binary Address								Hexa Address
	Decoder input and enable				Input to address pins of 8257				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Channel-0 DMA address register	0	1	1	0	0	0	0	0	60
Channel-0 count register	0	1	1	0	0	0	0	1	61
Channel-1 DMA address register	0	1	1	0	0	0	1	0	62
Channel-1 count register	0	1	1	0	0	0	1	1	63
Channel-2 DMA address register	0	1	1	0	0	1	0	0	64
Channel-2 count register	0	1	1	0	0	1	0	1	65
Channel-3 DMA address register	0	1	1	0	0	1	1	0	66
Channel-3 count register	0	1	1	0	0	1	1	1	67
Mode set register (Write only)	0	1	1	0	1	0	0	0	68
Status register (Read only)	0	1	1	0	1	0	0	0	68

Source : http://mediatoget.blogspot.in/2013/01/interfacing-of-8257-with-8085-processor.html