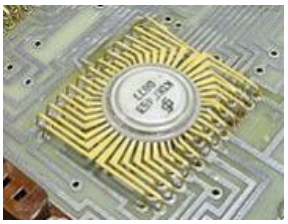
INTEGRATED CIRCUIT PACKAGING



Integrated circuit packaging is the final stage of semiconductor device fabrication per se, followed by IC testing.

In the integrated circuit industry it is called simply packaging and sometimes semiconductor device assembly, or simply assembly. Also, sometimes it is called encapsulation or seal, by the name of its last step, which might lead to confusion, because the term packaging generally comprises the steps or the technology of mounting and interconnecting of devices (see Chip carrier, Category:Chip carriers).

The earliest integrated circuits were packaged in ceramic flat packs, which continued to be used by the military for their reliability and small size for many years. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. In the 1980s pin counts of VLSI circuits exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages. Surface mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by small-outline integrated circuit — a carrier which occupies an area about 30 – 50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.

Small-outline integrated circuit (SOIC) and Plastic leaded chip carrier (PLCC) packages. In the late 1990s, plastic quad flat pack (PQFP) and thin small-outline packages (TSOP) became the most common for high pin count devices, though PGA packages are still often used for high-end

microprocessors. Intel and AMD are currently transitioning from PGA packages on high-end microprocessors to land grid array (LGA) packages.

Ball grid array (BGA) packages have existed since the 1970s. Flip-chip Ball Grid Array packages, which allow for much higher pin count than other package types, were developed in the 1990s. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a package substrate that is similar to a printed-circuit board rather than by wires. FCBGA packages allow an array of input-output signals (called Area-I/O) to be distributed over the entire die rather than being confined to the die periphery.

Traces out of the die, through the package, and into the printed circuit board have very different electrical properties, compared to on-chip signals. They require special design techniques and need much more electric power than signals confined to the chip itself.

When multiple dies are stacked in one package, it is called SiP, for System In Package, or three-dimensional integrated circuit. When multiple dies are combined on a small substrate, often ceramic, it's called an MCM, or Multi-Chip Module. The boundary between a big MCM and a small printed circuit board is sometimes fuzzy.

The following operations are performed at this stage.

The vast majority of integrated circuits are packaged in opaque ceramic or plastic insulation. The only connection to the outside world is through metal pins (sometimes called "leads") through the insulation.

The rare exceptions include proximity communication ; "blob on PCB" that attaches the raw die directly to a PCB,bonds the die wires directly to the PCB traces, then covers the die and the die wires with a blob of insulator; and partially or totally transparent packaging for optical input and/or output of optoelectronic devices and EPROM.

Source : http://en.pschitt.info/page/Integrated+Circuits