

FEATURES & FUNCTIONAL BLOCK DIAGRAM OF 8259 PROCESSOR

1. It is programmed to work with either 8085 or 8086 processor.
2. It manage 8-interrupts according to the instructions written into its control registers.
3. In 8086 processor, it supplies the type number of the interrupt and the type number is programmable. In 8085 processor, the interrupt vector address is programmable. The priorities of the interrupts are programmable.
4. The interrupts can be masked or unmasked individually.
5. The 8259s can be cascaded to accept a maximum of 64 interrupts.

FUNCTIONAL BLOCK DIAGRAM OF 8259:

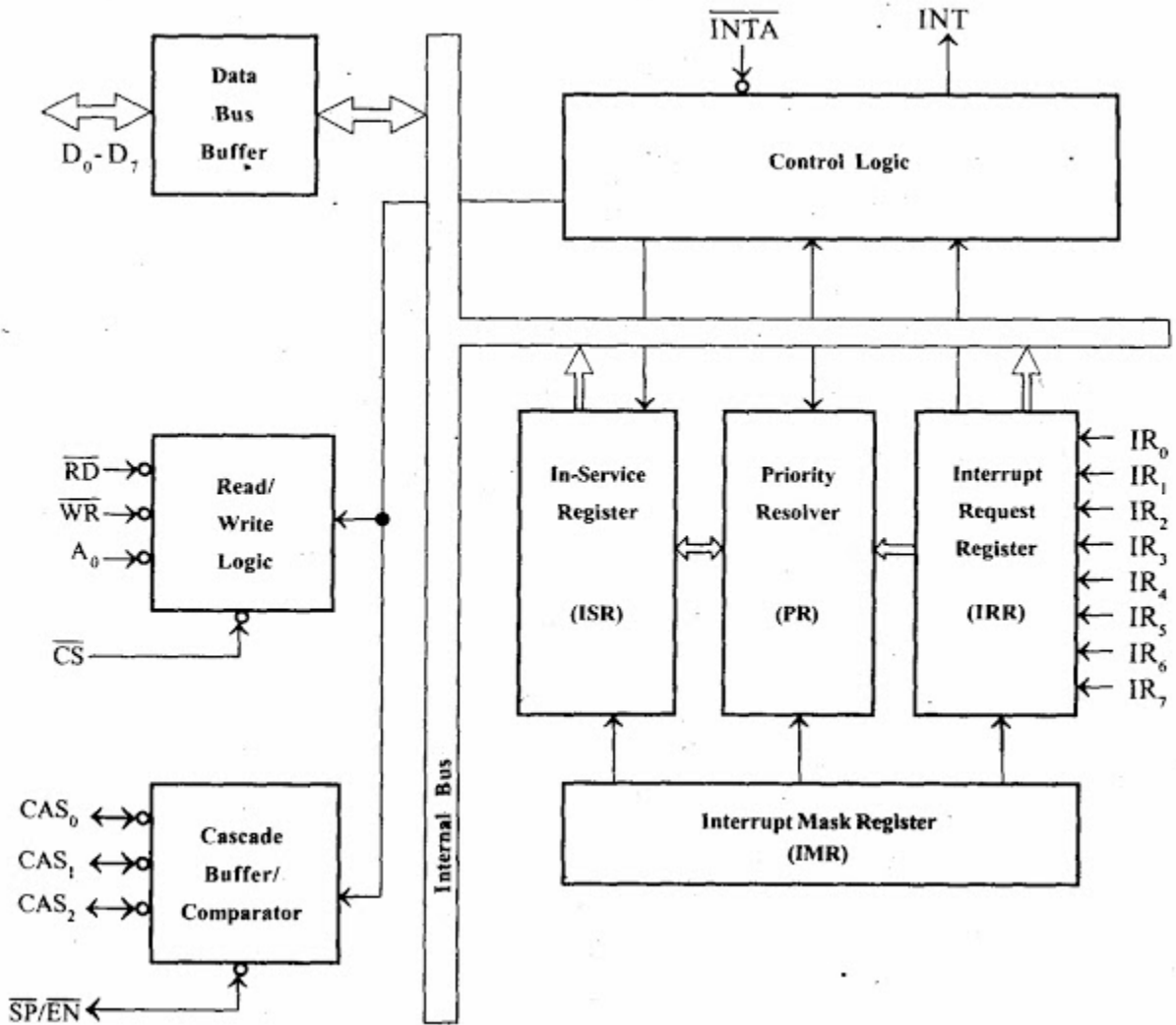
- It has eight functional blocks. They are,

1. Control logic
2. Read Write logic
3. Data bus buffer
4. Interrupt Request Register (IRR)
5. In-Service Register (ISR)
6. Interrupt Mask Register (IMR)
7. Priority Resolver (PR)
8. Cascade buffer.

The data bus and its buffer are used for the following activities.

1. The processor sends control word to data bus buffer through D0-D7.
2. The processor read status word from data bus buffer through D0-D7.

3. From the data bus buffer the 8259 send type number (in case of 8086) or the call opcode and address (in case of 8085) through D0-D7 to the processor.



- The processor uses the RD (low), WR (low) and A0 to read or write 8259.
- The 8259 is selected by CS (low).
- The IRR has eight input lines (IR0-IR7) for interrupts. When these lines go high, the request is stored in IRR. It registers a request only if the interrupt is unmasked.
- Normally IR0 has highest priority and IR7 has the lowest priority. The priorities of the interrupt request input are also programmable.

- First the 8259 should be programmed by sending Initialization Command Word (ICW) and Operational Command Word (OCW). These command words will inform 8259 about the following,

- * Type of interrupt signal (Level triggered / Edge triggered).

- * Type of processor (8085/8086).

- * Call address and its interval (4 or 8)

- * Masking of interrupts.

- * Priority of interrupts.

- * Type of end of interrupts.

- The interrupt mask register (IMR) stores the masking bits of the interrupt lines to be masked. The relevant information is sent by the processor through OCW.

- The in-service register keeps track of which interrupt is currently being serviced.

- The priority resolver examines the interrupt request, mask and in-service registers and determines whether INT signal should be sent to the processor or not.

- The cascade buffer/comparator is used to expand the interrupts of 8259.

- In cascade connection one 8259 will be directly interrupting 8086 and it is called master 8259.

- To each interrupt request input of master 8259 (IR0-IR7), one slave 8259 can be connected. The 8259s interrupting the master 8259 are called slave 8259s.

- Each 8259 has its own addresses so that each 8259 can be programmed independently by sending command words and independently the status bytes can be read from it.

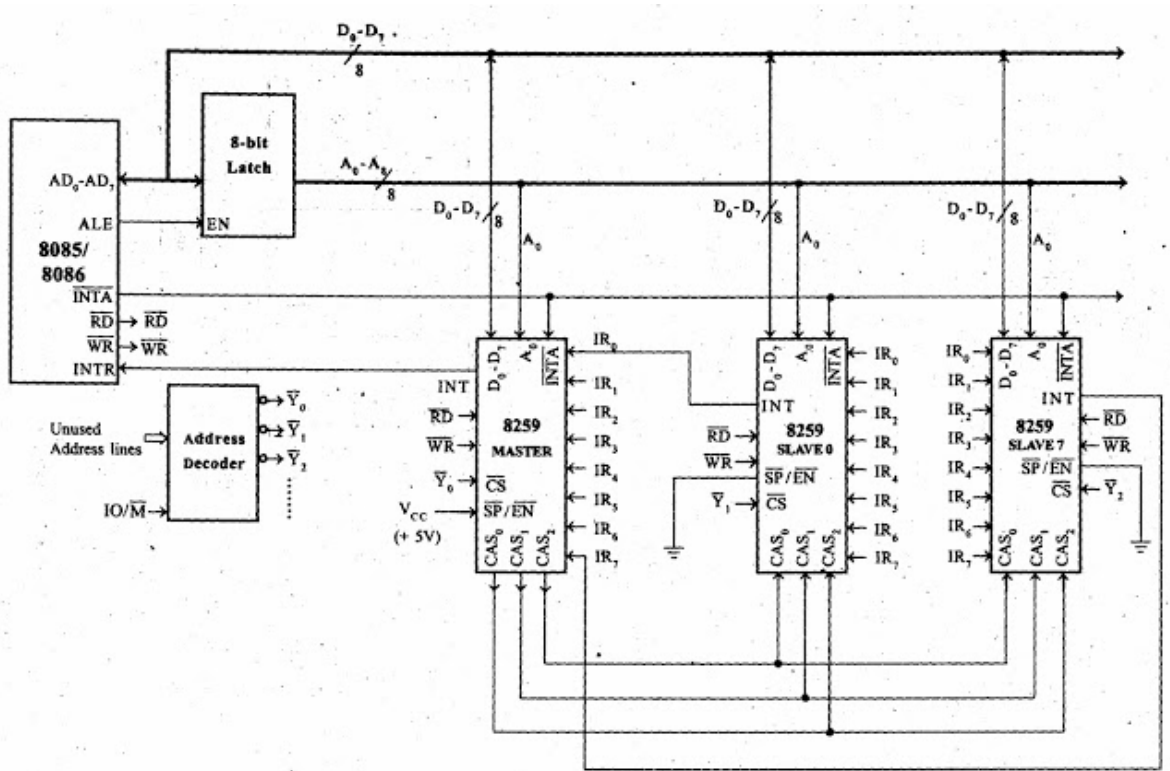
- The cascade pins (CAS0, CAS1 and CAS2) from the master are connected to the corresponding pins of the slave.

- For the slave 8259, the SP (low) / EN (low) pin is tied low to let the device know that it is a slave.

- The SP (low) / EN (low) pin can be used as input or output signal.

- In non-buffered mode it is used as input signal and tied to logic-1 in master 8259 and logic-0 in slave 8259.

- In buffered mode it is used as output signal to disable the data buffers while data is transferred from 8259A to the CPU.



Cascade Connection of 8059

Source : <http://mediatoget.blogspot.in/2013/02/features-functional-block-diagram-of.html>