FRACTIONAL-N FREQUENCY SYNTHESIZER DESIGN FOR RFAPPLICATIONS

MUDASSAR I. Y. MEER
Department of Electronics and Communication Engineering,
Indian Institute of Technology (IIT) Guwahati, Guwahati 781039,India
meer@iitg.ernet.in

AJAY KUMAR GUPTA
Department of Electronics and Communication Engineering,
Indian Institute of Technology (IIT) Guwahati, Guwahati 781039,India
g.ajay@alumni.iitg.ernet.in

ROY P. PAILY
Department of Electronics and Communication Engineering,
Indian Institute of Technology (IIT) Guwahati, Guwahati 781039,India
roypaily@iitg.ernet.in

Abstract:
In this work, design of Fractional-N Frequency Synthesizer using PLL has been investigated. The simulation is done in 0.18 μm CMOS technology with CADENCE tools using UMC foundry models. The different parts of synthesizer discussed in detail. Three different phase detector architectures are implemented. High speed TSPC DFF has designed to divide the frequency of GHz range. The prescalar is modified to have a delay of 80 ps only. For VCO, a multi layer inductor is used to save the area. The phase noise can be further reduced with a ΔΣ modulator in feedback loop. The designed frequency synthesizer targets RF applications like DVB-SH, WLAN, 802.11, bluetooth, cordless phones and remote control.

Keyword: VCO, TSPC DFF, phase detector.

I. Introduction

With the explosive growth of the wireless communication industry, research related to communication circuits and architectures has received a great deal of attention. The major challenges are low-cost, low-voltage, and low-power designs, which combine necessary performance with the ability to be manufactured economically in high volumes. Recently, there has been an additional emphasis on integration of heterogeneous parts that constitute a communication transceiver. Modern transceivers are expected to operate over a wide range of frequencies.

The term frequency synthesizer generally refers to an active electronic device that accepts some frequency reference (f_{ref}) input signal of a very stable frequency and then generates the desired frequency output, whereby the stability, accuracy, and spectral purity of the output correlate with the performance of the input reference.

In this article, we present the design of different blocks of fractional-N frequency synthesizer, which has the advantages over other frequency synthesizers. In fractional-N synthesizer the division ratio of Voltage Controlled Oscillator (VCO) frequency is fractional e.g. N + 1/4. Fig. 1 shows the basic blocks of fractional-N frequency synthesizer. Phase Frequency Detector (PFD) block will detect the phase difference between the reference frequency and the signal coming from VCO. It will generate UP or DOWN signal dependent on the lagging or leading of the reference frequency. The UP and DOWN signal will control the charge pump block. On UP signal the control voltage of VCO increase and decrease for DOWN signal. Loop filter is a low pass filter to get the ripple free controlled voltage. VCO will generate the sinusoidal signal depending on the controlled voltage. The frequency divider will divide the VCO frequency to the reference frequency.

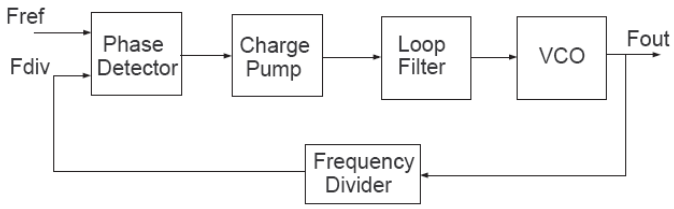

Fig. 1: Block diagram of Phase Locked Loop.

2. PFD Design

Phase frequency detector (PFD) is one of the important parts in PLL circuits. PFD is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. PFD has two outputs UP and DOWN which are signalled according to the phase and frequency difference of the input signals. The output signals of the PFD are fed to the Charge Pump (CP). The output voltage of the charge pump controls the output frequency of the VCO, so with a change happens at the input of the CP the output voltage will change which will change the output frequency of the VCO [1].

In this section we discussed the three types of PFD implementation i.e. Type I PFD, Modified Type I and Type II PFD. Fig. 2 shows the Type I PFD. Once CLKREF goes high it will charge the flip-flop and charges UP signal to high. When CLKVCO becomes high it will change DOWN signal to high. This will lead to have both output at high which will let AND gate to signal the reset output and reset both flip-flops driving both outputs to low. Since CLKREF is leading in Fig. 2, it is noticed that only UP signal is signalling when CLKREF change to high. In other case when the CLKVCO is leading, the opposite is true, which means DOWN signal will be high when CLKVCO change to high.

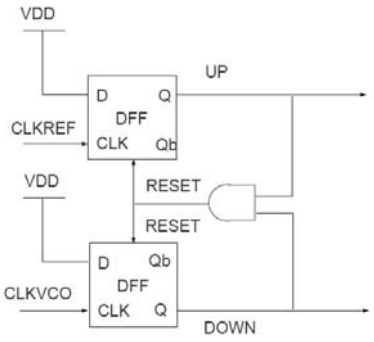

Fig. 2: Type I Phase Frequency Detector.

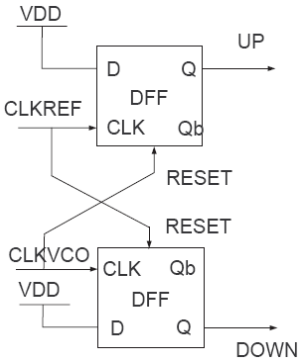

Fig. 3: Modified Type I Phase Frequency Detector.

The sensitivity of the phase and frequency difference detection of the PFD is very crucial. Sensitivity of the PFD means the smallest difference the PFD can detect and produce UP or DOWN signals that will affect the charge pump, this lead to the conclusion that the higher the sensitivity the better the PFD. One of the disadvantages that PFD suffers is dead-zone. Dead-zone is a small difference in the phase of the inputs that a PFD will not be able to detect. Dead zone is due to the delay time of the logic components and of the feedback path of the flip flops.

The problem with type I PFD is power consumption and the dead zone. Dead-zone is due to their small phase error. When the phase difference between PFDs input signals, the output signals of the PFD will not be proportional to this error [3]. It has 66.9 μW power dissipation with 80 ps dead zone. For reducing the power dissipation and dead zone Type I PFD is modified to set 9.81 μW power dissipation with 40 ps dead zone. In Modified Type I PFD, the reset path with AND gate is removed and DFF is set to reset directly with the respective CLK signal. Fig. 4 shows that at 40 ps delay the DOWN signal become low enough that it will not switch on the pull down transistor in the charge pump. It means that it has only 40 ps dead zone. For still reducing the power dissipation and dead zone the Type II PFD is preferred [2].

From Fig. 5, when CLKREF = ’0’ and CLKVCO become ’1’ then the node UP become high and node DOWN remains at low, now As CLKREF goes high the node UP will become low and node DOWN will be remain in low state. In another case when the CLKVCO = ’0’ and CLKREF goes high the node DOWN will become high and node UP will be at low state, now as the CLKVCO become high at the node DOWN will

become low and the node UP will be remain in low state. The other components in the design are NAND gate and inverter. Fig. 6 shows the dead zone curves for Type II PFD, which is only 15 ps, which corresponds to 0.0012π rad at 40 MHz reference frequency.

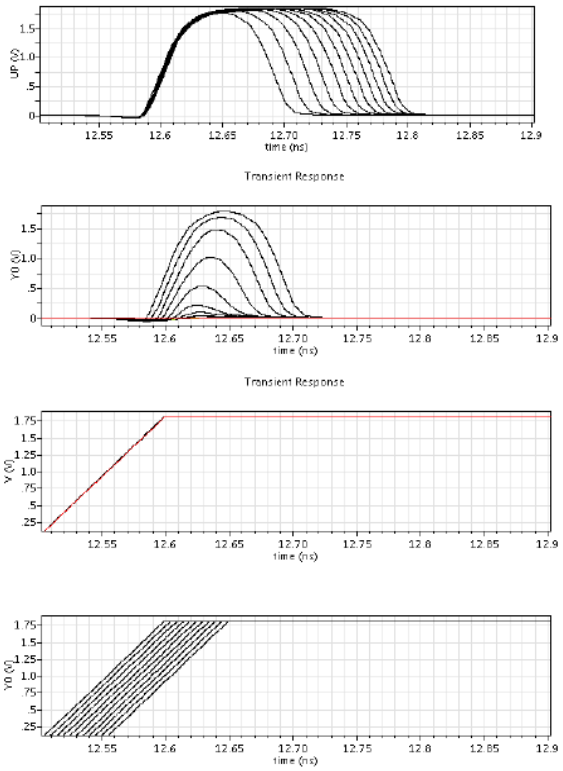

Fig. 4: Dead Zone for Modified Type 1 PFD.

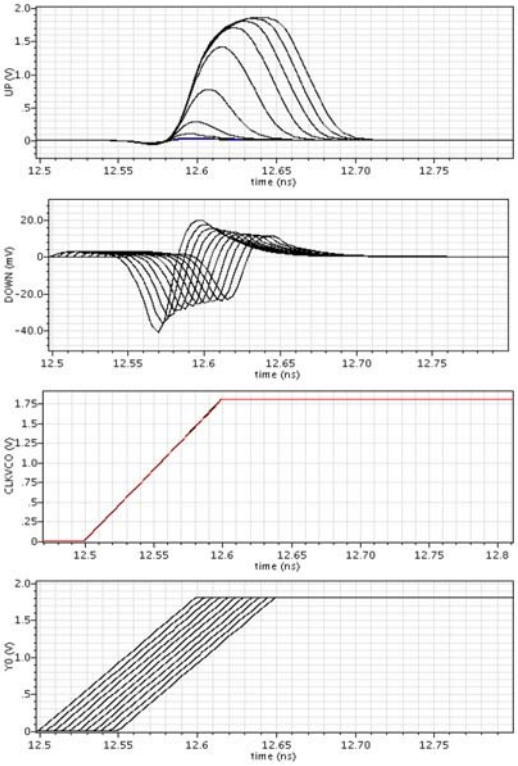

Fig. 6: Dead Zone for Type II PFD .

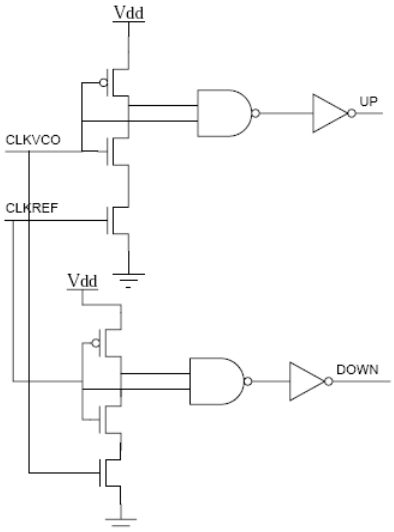

Fig. 5: Type II Phase Frequency Detector [2].

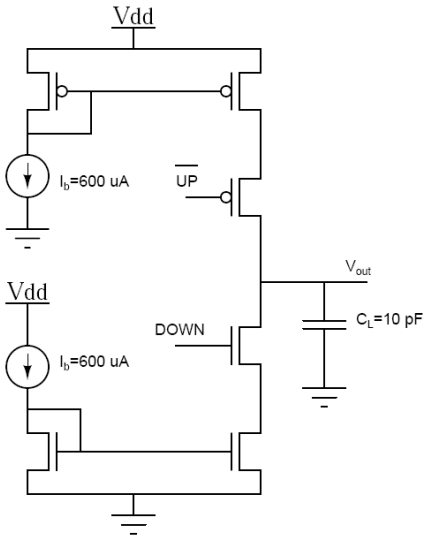

Fig. 7: Schematic Design of Charge Pump.

3. Charge Pump

Charge Pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. As shown in Fig. 7, charge pump consist of two switched current sources driving a capacitance load [4]. Charge pump is switched on and off by the PFD output signals UP and DOWN. This charge pump consists of two switched current sources that pump charge into or out of the loop filter according to the PFD output. When the reference leads the feedback signal, the PFD detects a rising edge on the reference frequency and it will produce an UP signal. This UP signal from the PFD will turn the UP switch (PMOS) on,

and it will cause the CP to inject current into the loop filter, increasing V_{out} . When the feedback leads the reference signal, the PFD detects a rising edge on the feedback signal and will produce a DOWN signal. This DOWN signal from the PFD will turn the DOWN switch (NMOS) ON, and the CP will sink current out of the loop filter thus, decreasing V_{out} . The current through the UP switch, and the current through the DOWN switch, need to be equal in order to avoid any current mismatch. The minimum charge pump current is limited by the switching speed requirements. Fig.8 shows the complete simulation result of phase detector with charge pump with 45^0 phase error. It shows that the capacitor is charging only when the UP is high, and will be stable if the UP and DOWN both are low and vice versa.

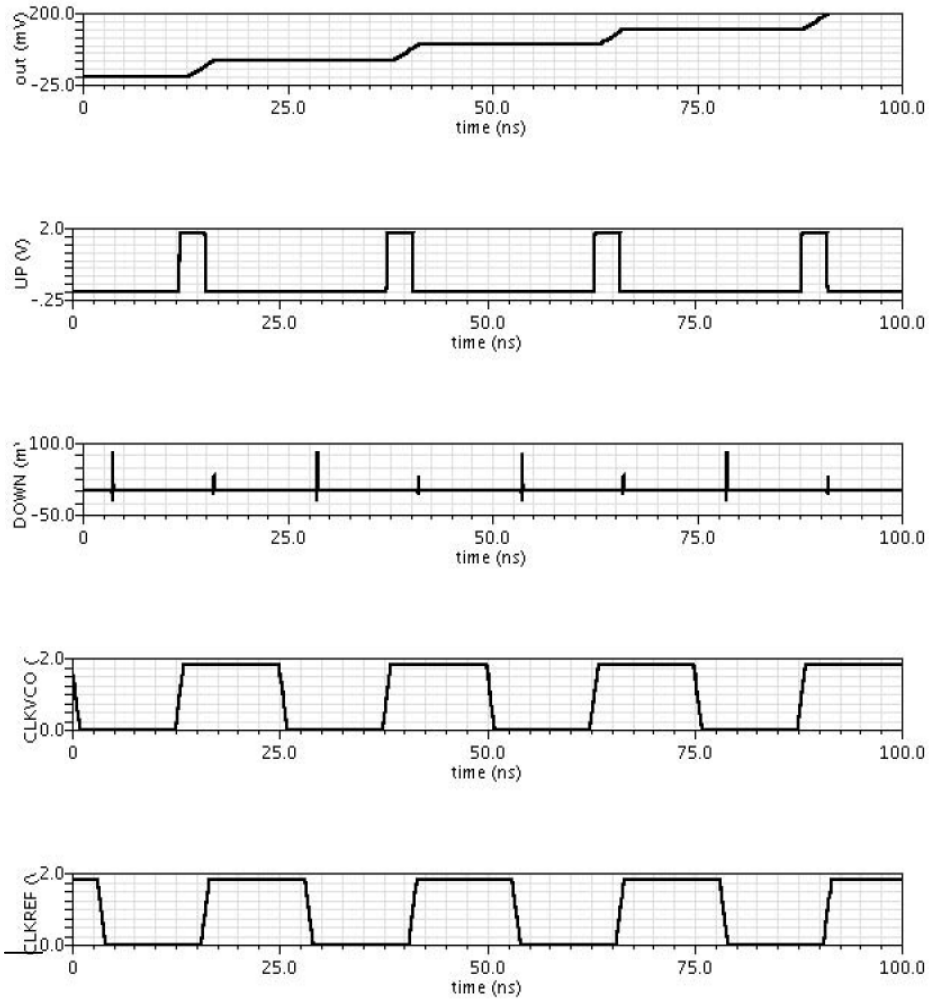

Fig. 8: PFD-CP Simulation for 45^0 phase error.

4. True Single Phase Clocked D-Flip Flop (TSPC DFF)

D-flip-flops with high-speed operation and low-power consumption are essential for high performance frequency synthesizers. Various flip-flops have been proposed to improve the operating speed of dual-modulus pre scalars. The dynamic D flip- flop designs in previous studies found suffer from glitch and charge-sharing problems [5] [6], which may result in incorrect operations. To alleviate these problems, additional transistors are introduced to some critical nodes to make these nodes stable [7] [8]. However, the newly added transistors limit operating speed and increase power consumption. In high-frequency operations, ratioed logic can replace ratio less logic without significant penalty on power consumption [9] [10]. Ratioed logic, however, consumes high power in low frequency operation, and their operating frequency range is limited.

Dynamic or clocked logic gates are used to decrease circuit complexity, increase operating speed, and lower power dissipation [11]. Of various dynamic CMOS circuit techniques, a true single-phase-clock (TSPC) dynamic CMOS circuit is operated with one clock signal that is never inverted. Therefore, no clock skew exists except for the clock delay problems, and even higher clock frequency can be achieved [12].

Fig. 9 shows a TSPC DFF for high-speed operation introduced in [13]. The flip-flop consists of nine transistors, where the clocked switching transistors are placed closer to power/ground for higher speed [14]. The

state transition of the flip-flop occurs at the rising edge of the clock signal, CLK. In Fig. 9, Qb becomes high when CLK changing low to high with D = 0. If D = 0 and CLK = 0, MPS1, MP1, and MPS2 are turned on and N1, Y1, and Y2 become high. If the signal CLK changes low to high, the node Y2 is discharged to low through MN2 and MNS1, making MP2 be on and Qb high. The analysis can be extended to other input combinations in the same manner.

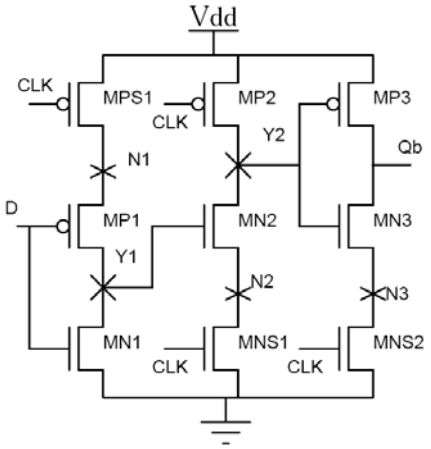

Fig. 9: A TSPC D-flip-flop for high-speed operation.

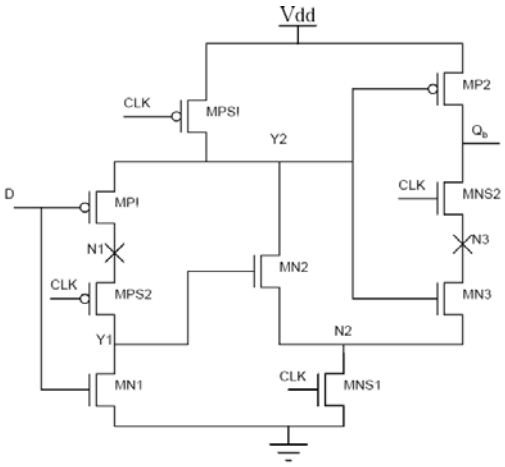

Fig. 10: D-flip-flop for glitch elimination [15].

Edge-triggered flip-flops take incoming data at the edge of a clock signal. Glitch problems may occur making the flip flops fall into wrong states. Consider Fig. 9 with CLK = 0 and D = 0, where Y1 and Y2 are pre-charged to high voltage. If CLK changes low to high, the node Y2 is discharged to low after some delay. In other words, Y2 remains high for a short time, in which MN3 and MNS2 are turned on and Qb may change to low. By discharging of Y2, then, Qb returns to the correct state of high. Consider the circuit in Fig. 9 in order to discuss charge sharing effects. When CLK is low, the node Y2 is always pre-charged high making MN3 on. The nodes, then, Qb and N3 may share their charges. The high level of Qb is somewhat lowered by sharing charges with the low level of N3.

Charge sharing raises more serious problems when the D flip-flop is used as a toggle-flip-flop operating in a lower frequency range. For toggle operations, Qb is tied to D. By changing CLK low to high with Qb in a high state, Qb toggles to low. Since Qb and D are tied together, D is forced to change high to low right after CLK changes low to high. The time that D stays low is almost half the period of CLK. In a lower operating frequency, Y2 would have enough time to discharge making MP2 turn on strongly and Qb high. The flip-flop, therefore, loses its edge-triggering characteristics and fails to perform proper operations.

Transistor merging technique is used to reduce the number of transistors and thereby save both power and silicon area while suppressing glitch occurrences. Pull-up and pull-down transistors are combined together yielding a circuit having fewer pull-up and pull-down transistors. Consider the circuit shown in Fig. 9, where the nodes n1 and y2 have the same potential of VDD during CLK = 0. When CLK = 1, its operation is independent of the N1 level and Y2 may stay high or discharge to low. This observation leads to merge two pullup transistors of the conventional design. MPS1 and MPS2 in Fig. 9 are merged to MPS1 as shown in Fig. 10. With the same analysis, MNS1 in Fig. 10 replaces MNS1 and MNS2 in Fig. 9.

Consider the circuit of Fig. 10, where nodes Y1, N1, and Y2 are pre-charged high with CLK = 0 and D=0. During this phase, MNS1 and MP2 are off, and Qb holds the previous value. Note that both N2 and N3 are weak high because of Y1 and Y2 being high. Assuming that CLK changes low to high, MPS1 and MPS2 are turned off and MNS1 and MNS2 are on. Since Y2 cannot discharge instantly, a pull-down path is formed consisting of MNS2, MN3, and MNS1. But N2 and N3 keep weak high from the previous phase resulting in a small glitch due to the voltage drop of Qb. As Y2 becomes low through MN2 and MNS1 path, Qb rises high.

Considering that CLK = 0 and D = 1 in Fig. 10, Y2 is pre-charged to high but Y1 is low. This makes MN2 be turned off. If CLK changes low to high, Qb discharges low through the path consisting of MNS2, MN3, and MNS1. If we change D to low when CLK = 1, MP1 is turned on, but the charge sharing between Y1 and Y2 never occurs due to the blocking transistor MPS2. This implies that MN2 remains off and the pull-down path of node Y2 does not exist.

Though there exists the charge sharing effect between Y2 and N1, but it's not severe as in Fig. 10. After charge sharing Y2 has a stable final value, since CLK = 1 and MN2 is off. On the other hand, the charge sharing in Fig. 10 turns on MN2, and Y2 continues to discharge. The voltage drop of Y2 resulting from charge sharing between N1 and Y2 is determined by the ratio of the total capacitance of N1 and Y2. Fig. 11 shows the output of TSPC DFF. Here the glitches of only 2.5% of power supply can be observed.

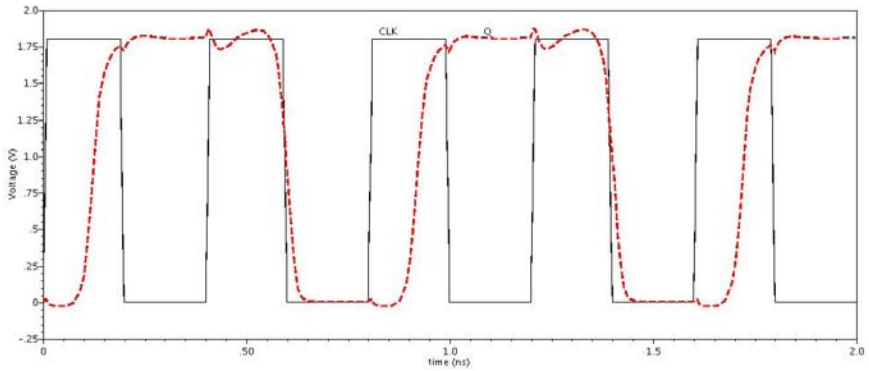

Fig. 11: Transient response of TSPC DFF used as TFF.

5. Dual Modulus Prescalar

Fig. 12 illustrates the block diagram of a typical divided by N or N+1 dualmodulus prescalar. It consists of a divided by 4 or 5 counter (in the dashed-line box), several divided by- 2 toggle flip-flops (TFF) and a few logic gates. The dual modulus prescalar is used in a fractional-N phase-locked loop, in which the MODE pin is controlled by an accumulator or a sigma-data modulator. By changing the ratio of 0s and 1s on the MODE pin, one can obtain a fractional division number between N and N+1 [16]. The operation mode is further explained below.

When MODE is set to ’0’, the output of the 5-input NAND gate is always ’1’., and will not be influenced by the output of the TFF chain. This implies that the output of the NOR gate in the divided-by-4/5 stays at ’0’, and therefore the Qb pin of the succeeding DFF stays at ’0’. As a result, the first two DFFs are isolated from the third DFF, and they form a divided by- 4 counter. The divided-by-4 counter is further fed to the TFF chain of a divided-by-16 divider. The total division ratio is therefore 64. Fig. 13 shows the output of prescalar. When the MODE = 0, the division ratio is 64, and when the MODE = 1 and all other input to the NAND gate is 1, then the division ratio is 65.

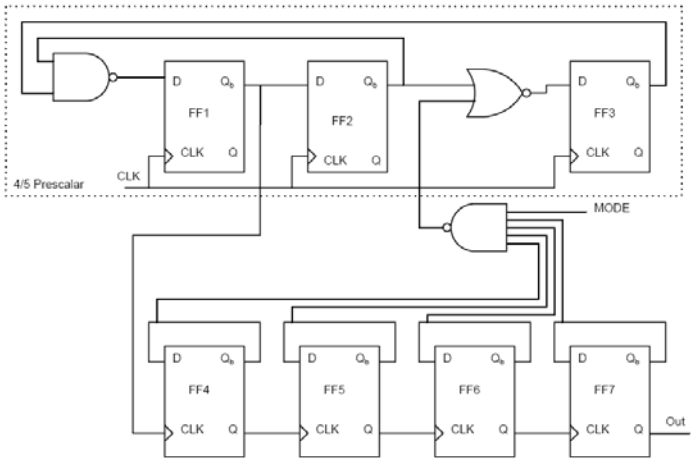

Fig. 12: Block diagram of dual-modulus (64/65) prescalar .

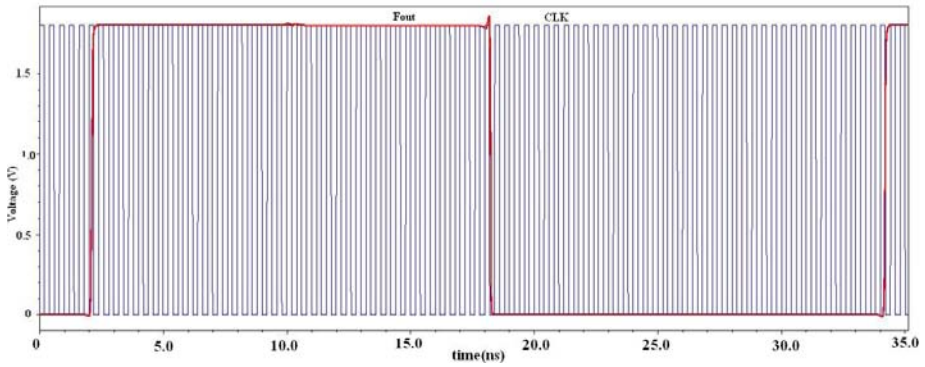

Fig. 13: Output of (64/65) prescalar.

6. Designing Voltage Controlled Oscillator (VCO)

The design of LC oscillator is shown in Fig. 14. Multilayer inductor [17] is use in VCO design to reduce the area. The PMOS in inversion mode is used as varactor. Fig. 15 shows the frequency variation of VCO with respect to V_{tune}. Here the response is almost linear in the region of 0.9 - 1.8 V i.e. from 2.545 - 2.370 GHz. The frequency sensitivity is 195 kHz/mV. Fig. 16 shows that the phase noise for this VCO is -118 dBc/Hz at 1 MHz. Settling time for the VCO is 2 ns, which is not bad. Here the phase noise in only -118 dBc/Hz which can be improved by phase reduction techniques. Fig. 17 shows the layout of designed VCO.

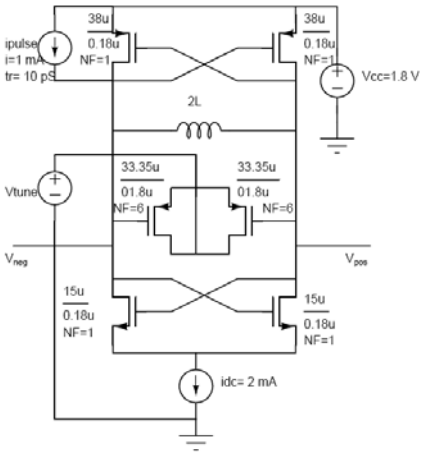

Fig. 14: Detailed VCO circuit diagram.

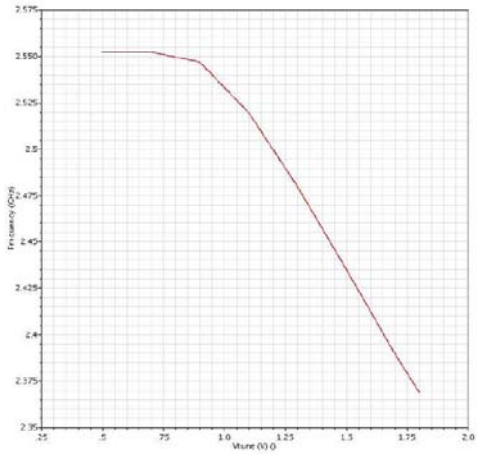

Fig. 15: Frequency variation of VCO Vs. Tuning Voltage Curve.

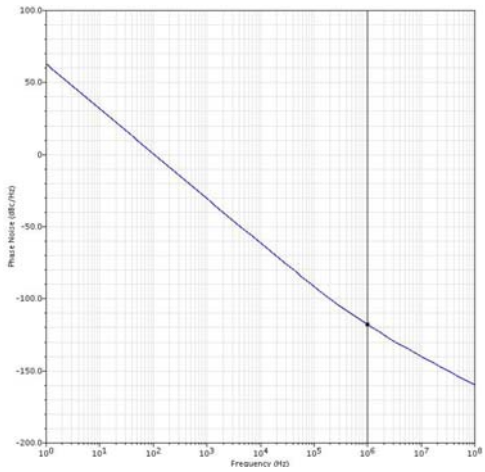

Fig. 16: Phase Noise plot of designed VCO.

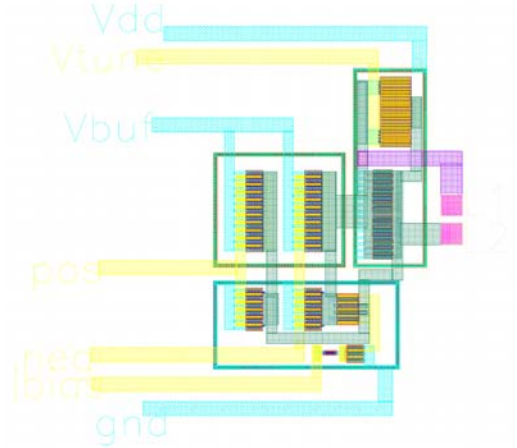

Fig. 17: Layout of VCO.

7. Conclusion

In this work the design steps required to build a Fractional- N Frequency Synthesizer using PLL are investigate. Different architecture of DFF is used to reduce the power consumption in Phase/Frequency Detector. The Phase/Frequency Detector of first type has power dissipation of 9.81 μW at 40 MHz and the dead zone of 40 ps. While the type 2 Phase/Frequency Detector have power dissipation of 6.228 μW at 40 MHz and the dead zone of 15 ps which is equal to 0.0012π. High speed TSPC DFF has designed to divide the frequency of GHz range. The area of designed TSPC DFF is 34 μm X 27 μm. The design of VCO is carried out in 0.18 μm technology using multilayer inductor to save the area. Area for the designed VCO is 80 μm X 100 μm. The phase noise of VCO is -118 dBc/Hz at 1 MHz. The phase noise of system can be still reduce after applying some phase noise reduction techniques, such as ΔΣ Modulator in feedback loop.

References

[1] Chou, Chien-Ping, Lin, Zhi-Ming,and Chen, Jun-Da, "A 3-ps dead-zone double-edge-checking phase-frequency-detector with 4.78 GHz operation frequency," The 2004 IEEE Asia-Pacific Conference on Circuits and Systems conference, vol. 2, pp. 937–940, 2004.

[2] Chou, Chien-Ping, Lin, Zhi-Ming, and Chen, Jun-Da, "A 3 ps dead-zone double-edge-checking phase-frequency-detector with 4.78 GH operation frequency," The 2004 IEEE Asia-Pacific Conference on Circuits and Systems conference, vol. 2, pp. 937–940, 2004.

[3] Barrett, Curtis, Fractional/ Integer-N PLL Basics. Texas Instruments, Wireless Communication Business Unit, August 1999.

[4] Juarez-Hernandez and Alejandro Diaz-Sanchez, "A novel CMOS charge pump circuit with positive feedback for PLL applications," The 8th IEEE International Conference on Electronics, Circuits and Systems, vol. 1,pp. 349–352, 2001.

[5] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," IEEE Journal Solid-State Circuits, vol. 24, pp. 62–70, Feb. 1989.

[6] R. Rogenmoser, N. Felber, Q. Huang, and W. Fichtner, "1.16 GHz dual-modulus 1.2 μm CMOS prescaler," Proc. IEEE 1993 CICC, p. 27.6.127.6.4, May 1993.

[7] Q. Huang and R. Rogenmoser, "A glitch-free single-phase DFF for gigahertz applications," Proc. IEEE 1994 ISCAS, vol. 4, pp. 11–13, May 1994.

[8] R. Rogenmoser, Q. Huang, and F. Piaza, "1.57 GHz asynchronous and 1.4 GHz dual-modulus 1.2 μm CMOS prescaler," Proc. IEEE 1994 CICC, pp. 387–390, May 1994.

[9] B. Chang, J. Park, and W. Kim, "A 1.2 GHz CMOS dual modulus prescaler using new dynamic D-type flip-flops," IEEE Journal Solid-State Circuits, vol. 31, pp. 749–752, May 1996.

[10] C.-Y. Yang, G-.-K. Dehng, J.-M. Hsu, and S.-I. Liu, "New dynamic flip flops for high-speed dual-modulus prescaler," IEEE Journal Solid-State Circuits, vol. 33, pp. 1568–1571, Oct. 1998.

[11] R.J. Baker, H.W. Li, and D.E. Boyce, CMOS Circuit Design, Layout, and Simulation. IEEE Press, New York, 1998.

[12] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, pp. 62–70, Feb. 1989.

[13] H. Oguey and E. Vittoz, "CODYMOS frequency dividers achieve low power consumption and high frequency," Electron Lett., pp. pp.386–387, Aug. 1973.

[14] Q. Huang and R. Rogenmoser, "Speed optimization of edge triggered CMOS circuits for gigahertz single-phase clocks," IEEE J. Solid-State Circuits, vol. 31, pp. 456–465, March 1996.

[15] Sung-Hyun YANG, Younggap YOU, Kyoung-Rok CHO, "A new dynamic d-flip-flop aiming at glitch and charge sharing free," IEICE TRANS. ELECTRON., vol. E86-C, No. 3, pp. 496–505, March 2003.

[16] B. Miller and R. Conley, "A multiple modulator fractional divider," IEEE Transactions on Instrumentation and Measurement, vol. 40, pp. 578– 583, June 1991.

[17] Genemala Haobijam and Roy Paily, "Multilevel symmetric spiral inductor with reduced area and higher self resonating frequency," Indian Microelectronics Society (IMS) Conference, Aug. 2007.