

DYNAMIC VS STATIC TIMING ANALYSIS

Timing analysis is integral part of ASIC/VLSI design flow. Anything else can be compromised but not timing! Timing analysis can be **static** or **dynamic**. Dynamic timing analysis verifies functionality of the design by applying input vectors and checking for correct output vectors whereas Static Timing Analysis checks static delay requirements of the circuit without any input or output vectors.

Dynamic timing analysis has to be accomplished and functionality of the design must be cleared before the design is subjected to Static Timing Analysis (STA). Dynamic Timing Analysis (DTA) and Static Timing Analysis (STA) are not alternatives to each other. Quality of the Dynamic Timing Analysis (DTA) increases with the increase of input test vectors. Increased test vectors increase simulation time. Dynamic timing analysis can be used for synchronous as well as asynchronous designs. Static Timing Analysis (STA) can't run on asynchronous designs and hence Dynamic Timing Analysis (DTA) is the best way to analyze asynchronous designs. Dynamic Timing Analysis (DTA) is also best suitable for designs having clocks crossing multiple domains.

Example of Dynamic Timing Analysis(DTA) tool is Modelsim (from mentor Graphics), VCS (from Synopsys). DTA is also carried out on post layout netlist to verify that functionality of the design has not changed. Test vectors remain same for both.

SPICE Simulation

Device level timing analysis is carried out using SPICE simulation. SPICE simulation is very essential for full custom designs to verify the electrical properties of the designs. These are calculated based on the mathematical equations that represent electrical properties of devices. Material and some of the electrical properties of the devices, which are represented by either variables or constants, are stored in model files. Examples are threshold voltage of MOSFET, electron density etc. SPICE characterized data is tabulated in technology libraries which becomes basic delay information for the Static Timing Analysis. For example let us consider a AND gate. Several electrical properties such as input and output transition, propagation delay, output capacitance etc are evaluated by this SPICE simulation. SPICE simulated data gives maximum accuracy compared to any other form of simulation. SPICE code is manually written and simulated. Hence for a larger design SPICE simulation is cumbersome job. There are specific tools available for transistor level

Static Timing Analysis (STA), (Eg. Pathmill from Synopsys) SPICE simulation being the backbone of all these tools.

What is Static Timing Analysis (STA)?

In Static Timing Analysis (STA) static delays such as gate delay and net delays are considered in each path and these delays are compared against their required maximum and minimum values. Circuit to be analyzed is broken into different timing paths constituting of gates, flip flops and their interconnections. Each timing path has to process the data within a clock period which is determined by the maximum frequency of operation. Cell delays are available in the corresponding technology libraries. Cell delay values are tabulated based on input transition and fanout load which are characterized by SPICE simulation. Net delays are calculated based on the Wire Load Models(WLM) or extracted resistance R and capacitance C. Wire Load Models(WLM) are available in the Technology File. These values are Table Look Up(TLU) values calculated based on the net fanout length.

The static timing analyzer will report the following delays (or it can do following analysis):

Register to Register delays

Setup times of all external synchronous inputs

Clock to Output delays

Pin to Pin combinational delays

Different Analysis Modes-Best, Worst, Typical, On Chip Variation (OCV)

Data to Data Checks

Case Analysis

Multiple Clocks per Register

Minimum Pulse Width Checks

Derived Clocks

Clock Gating Checks

Netlist Editing

Report_clock_timing

Clock Reconvergence Pessimism

Worst-Arrival Slew Propagation

Path-Based Analysis

Debugging Delay Calculation

and many more.....!!

The wide spread use of STA can be attributed to several factors [David]:

- The basic STA algorithm is linear in runtime with circuit size, allowing analysis of designs in excess of 10 million instances.
- The basic STA analysis is conservative in the sense that it will over-estimate the delay of long paths in the circuit and under-estimate the delay of short paths in the circuit. This makes the analysis "safe", guaranteeing that the design will function at least as fast as predicted and will not suffer from hold-time violations.
- The STA algorithms have become fairly mature, addressing critical timing issues such as interconnect analysis, accurate delay modeling, false or multi-cycle paths, etc.
- Delay characterization for cell libraries is clearly defined, forms an effective interface between the foundry and the design team, and is readily available. In addition to this, the Static Timing Analysis (STA) does not require input vectors and has a runtime that is linear with the size of the circuit [Agarwal].

Advantages of STA:

- All timing paths are considered for the timing analysis. This is not the case in simulation.

- Analysis times are relatively short when compared with event and circuit simulation.
- Timing can be analyzed for worst case, best case simultaneously. This type of analysis is not possible in dynamic timing analysis.
- Static Timing Analysis (STA) works with timing models. STA has more pessimism and thus gives maximum delay of the design. DTA performs full timing simulation. The problem associated with DTA is the computational complexity involved in finding the input patterns (vectors) that produce maximum delay at the output and hence it is slow.

Disadvantages of STA:

- All paths in the design may not run always in worst case delay. Hence the analysis is pessimistic.
- Clock related all information has to be fed to the design in the form of constraints.
- Inconsistency or incorrectness or under constraining of these constraints may lead to disastrous timing analysis.
- STA does not check for logical correctness of the design.
- STA is not suitable for asynchronous circuits.

Source : <http://asic-soc.blogspot.in/2008/08/dynamic-vs-static-timing-analysis.html>