Design of Variable Width Barrel Shifter for High Speed Processor Architecture

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Abstract

Microprocessor is the brain of the computer. It works as the Central Processing Unit of the computer. It contains Arithmetic Logical Unit (ALU) that performs the arithmetic operations such as Addition, Subtraction, Multiplication and Division. It also performs the Logical operations such as AND, NAND, OR, NOR, EXOR, EXNOR and NOT. It also contains register file to store the operand in load/store instructions in RISC Processor Architecture. Control Unit genetares the control signals that synchronize the operation of the processor which tells the microarchitecture which operation is done at which time. Now during the multiplication partial product is shifted and added. So shifter is an important part of the processor architecture. Barrel Shifter is an important combinational logic block. It was incorporated in 386 processor and is also used in microcontroller design. Intel has since moved to software implemented shifters in the Pentium 4 Processor Architecture but AMD still uses it.

Here the design of the variable width barrel shifter is presented in which we can shift 4bit, 8bit, 16bit, and 32bit and maximum 64bit partial product during multiplication. Functionality is check using Modelsim 6.4a.Now to generate the gate level netlist Xilinx ISE 9.2i is used.

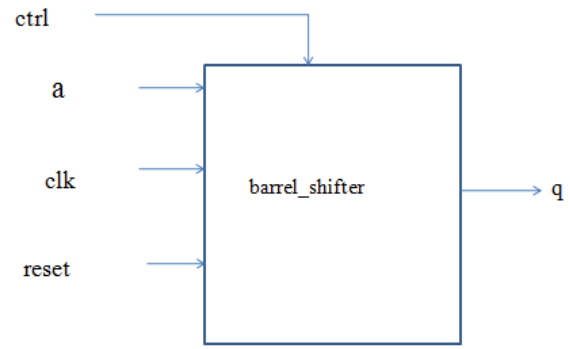
Keywords: RISC Processor, 386 Processor, AMD, Shift, Partial Product, Clock Latency

Experimental Work

Specifications are written first. Then they are converted into RTL.At this level of abstraction design is independent of technology. Now to define the technology Synthesis is required that creates netlist.Nelist is the electrical connectivity of the circuit. In the present design RTL coding is done in Verilog HDL Language. To check the functionality Simulation is done on Modelsim 6.4a.Present architecture shift maximum 64bits at a time.

Architecture Design

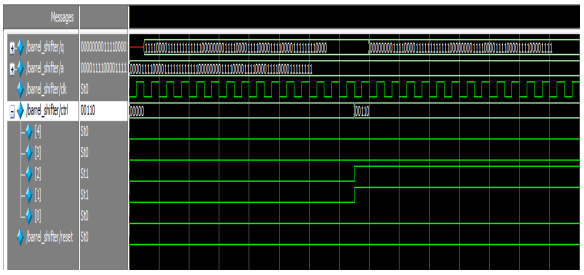
Here a is the variable width input, clk is the clock input and q is the output. Now for fast triggering negative edge clock is used with 50% duty cycle. Here the frequency of the clock is 10MHz.reset is the reset input used for initialization of shifter.



Encoding

Operation	Encoded word
Left shift by 4	00000
Left shift by 8	00001
Left shift by 16	00010
Left shift by 32	00011
Left shift by 64	00100
Right Shift by 4	00101
Right Shift by 8	00110
Right Shift by 16	00111
Right Shift by 32	01000
Right Shift by 64	01001

Simulation Result



Synthesis Report

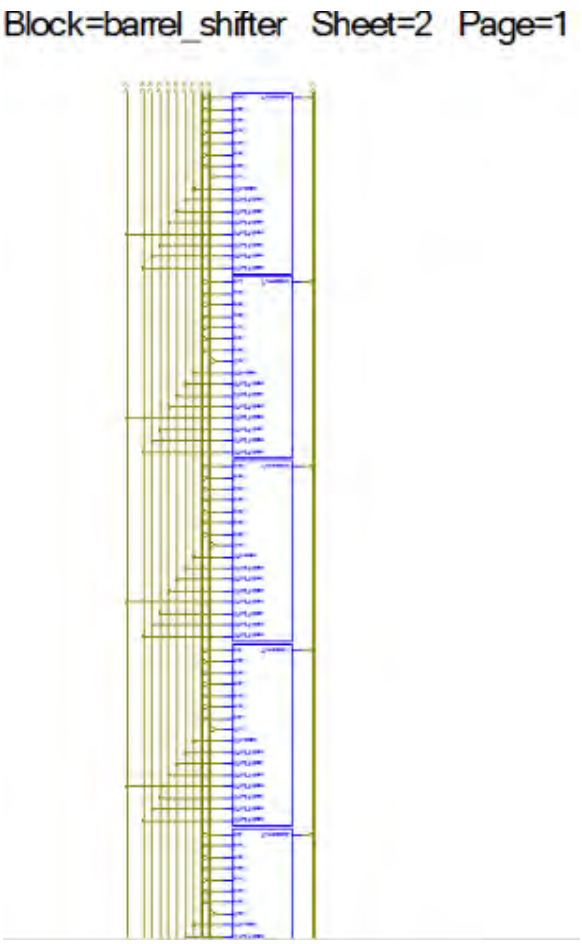
The present design is transferred on various FPGA depending upon the optimization of speed and power consumption.

The different parameters are given in the following table.

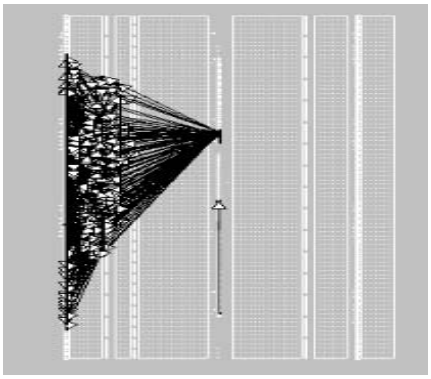
FPGA Type	**SPARTAN 2**	**SPARTAN 3**	**SPARTAN 3A**	**Virtex 5**	**Virtex E**	**Virtex 2**	**Virtex 2Pro**
Speed	281.770MHz	487.936MHz	611.639MHz	1280.902MHz	372.301MHz	611.803MHz	800.480MHz
Setup Time	19.591ns	3.484ns	7.357ns	3.484ns	13.648ns	6.094ns	5.459ns
Hold Time	6.959ns	6.280ns	5.271ns	2.527ns	5.967ns	4.711ns	3.340ns
Gate Delay	3.549ns	2.049ns	1.635ns	0.781ns	2.686ns	1.635ns	1.249ns
Net Delay	2.343ns	1.281ns	1.253ns	0.429ns	1.766ns	1.089ns	0.853ns
Clock Fanout	64	64	64	61	64	64	64
Power Consumption	13mW	491mW	182Mw	10621mW	7mW	98mW	98mW

Final implementation is done on **Virtex 5 FPGA** for High Speed. To obtain Low Power Consumption SPARTAN2 FPGA is required. But our aim is to find the architecture that provides high speed. So Virtex 5 FPGA is used for final implementation. In this case the shifter are operated at 1280.902MHz i.e. 1.28 GHz clock frequency. After simulation is over we find that clock latency is 12.Clock skew is 0.707ns.

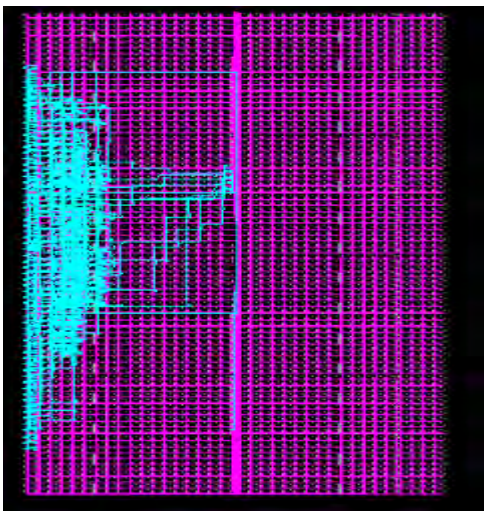
RTL Schematic



Chip Floorplan



Chip Design



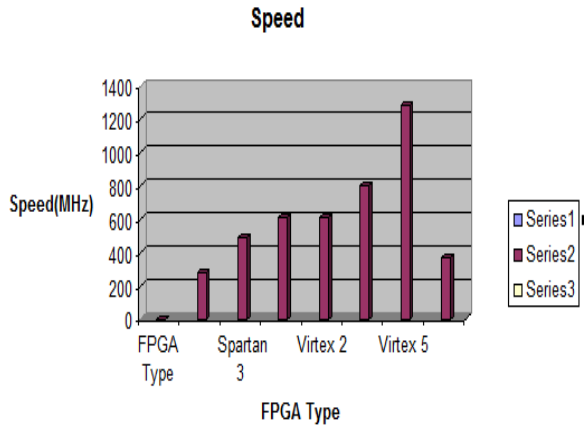
Final implementation is done on Virtex 5 FPGA with device xc5vlx30, package ff676 with speed grade -3.The final design consumes 10621mW power from the power supply. But the operating speed lies in GHz range. That is the optimization goal here. Here the Gate Count is 2016 and additional JTAG Gate Count for IC Testing is 6480.The final IC Package contains 216 bonded IO.

Conclusion

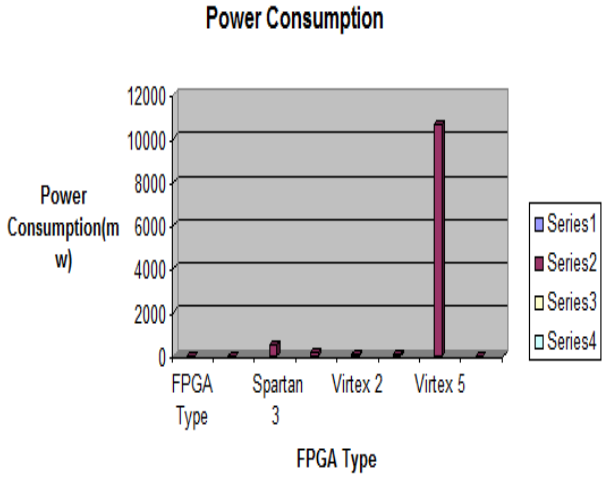
The present architecture provides the high speed. In future the architecture can be modified for low chip area to minimize the fabrication cost.

Similarly to increase the speed and to reduce the power consumption architecture should be pipelined.

Speed

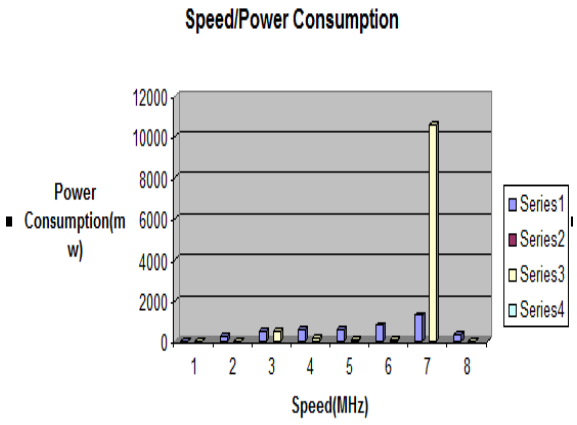


Power Consumption



Speed/Power Consumption

As shown from the following graph that as the operating speed of the circuit increases then power consumption will also increases.



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