High-Q RF coils on silicon integrated circuits

Christopher L. Chua[+], David K. Fork, Koenraad Van Schuylenbergh, Jeng-Ping Lu
Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304

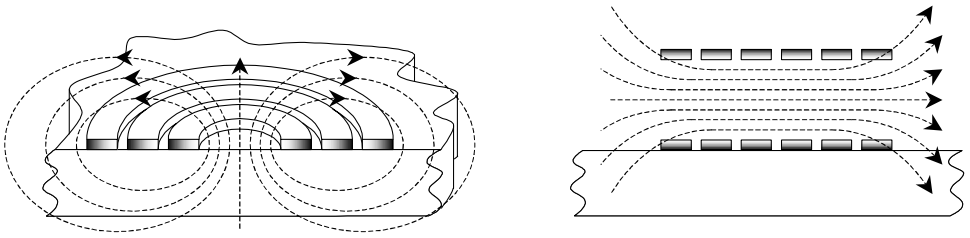
ABSTRACT

We report on out-of-plane micro-machined inductors exhibiting record high quality factors (Q) on silicon integrated circuits. The coils are made by three-dimensional self-assembly of stress-engineered structures fabricated with standard semiconductor batch processing techniques. Coils fabricated on low resistance CMOS-compatible silicon exhibit quality factors of over 70 at 1 GHz. BiCMOS test oscillators utilizing these micro-machined coils show significant phase noise reduction over similar oscillators using conventional spiral coils.

1. INTRODUCTION

High Q coils that can be integrated on silicon circuits have been an elusive goal for many years. Today, many radio-frequency integrated circuits (RFICs) requiring high performance inductors rely on off-chip discrete coils. Some circuits are even built from discretes in a modular assembly. Integrated high Q coils, if available, can transform the economics, size and power consumption of many RF circuits.

The Q-factor of current state-of-the-art inductors on conventional unaltered CMOS silicon is about 10. This low Q is attributed to fundamental limitations associated with coil designs involving variations of the pancake configuration shown in Figure 1a[1,2]. With the coil axis perpendicular to the wafer surface, large amounts of magnetic flux penetrate the substrate and induce lossy eddy currents. In addition to substrate losses, pancake coils have high alternating current (AC) resistances due to skin effect. During operation the magnetic field pushes AC current away from the field lines towards the outer skin of the conductor. As shown in Figure 1a, the current crowds along the outer edges of the coil windings causing high AC resistance. Widening the traces simply increases the unused portion of the conductor and does not reduce current crowding because the skin depth is independent of winding width.



(a) (b)

Figure 1: (a) Magnetic field and AC current distribution in a pancake spiral coil and (b) magnetic field and AC current distribution in an out-of-plane coil. Darker shadings on the windings indicate higher current densities.

[+] christopher.chua@parc.com; (650) 812 4113

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In this paper, we report on a new approach for batch fabricating low-loss coils on integrated circuits. Our design is based on an out-of-plane coil geometry shown in Figure 1b. Unlike pancake coils, few magnetic field lines penetrate the substrate, so fewer eddy currents are induced. In this geometry, the skin effect pushes the coil current to the outer surface of the winding rather than to the winding's edge. Therefore, a low trace resistance can be attained by simply widening the traces.

Our devices are constructed using stress-engineered thin films. The films are sputter-deposited with a built-in stress gradient so that, when patterned and released from their substrate, they curl into a designed radius of curvature. These micro-machined springs self-assemble into three-dimensional scaffolds that we electroplate with copper to form highly conductive coil windings.

2. MICRO-MACHINED SPRINGS

Stress engineering is accomplished by controlling the ambient pressure of the sputter chamber during film deposition. Many refractory metals have a common property of acquiring tensile stress when sputtered at high pressures and compressive stress when sputtered at low pressures. At low ambient pressures, sputtered atoms encounter few collisions before reaching the substrate. These energetic atoms tend to pack tighter than their natural arrangement. The tighter atomic arrangement forms compressively stressed films that prefer to expand when "released". The ambient argon atoms also hit the film with more energy, peening the film and adding to the compressive stress. Conversely, at high pressures, sputtered atoms loose most of their energy through collisions with ambient atoms before reaching the substrate surface. The sputtered atoms do not have sufficient energy to orient fully to their preferred natural arrangement. Consequently, they tend to form arrangements that are further spaced than normal. The film becomes tensile and contracts when released.

A stress gradient can be induced by simply changing the ambient pressure during film deposition. A film that is compressive at the bottom and tensile on the surface can, for example, be realized by increasing the pressure during sputtering. In practice, this pressure control is accomplished by flowing Argon and widening or narrowing an orifice opening to the pump. When patterned and released, such a stress-graded film curls up as shown in Figure 2. Our devices employ a molybdenum-chromium (MoCr) alloy for the stress-engineered layer. The exact stress-versus-pressure relationship is a function of the specific sputter tool geometry, the type of substrate used, and other process parameters that have to be characterized for each particular tool setup. Figure 2 shows sets of springs arranged in pairs oriented opposite each other.

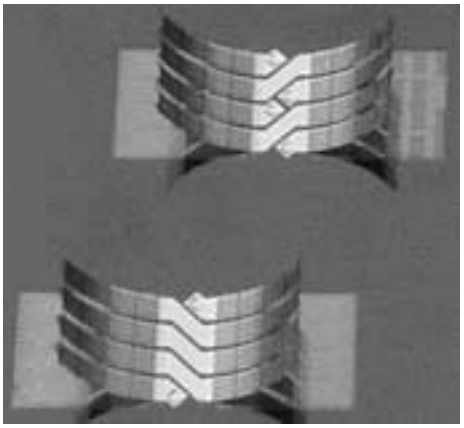

Figure 2: Released stress-engineered micro-machined springs

3. MICRO-MACHINED OUT-OF-PLANE INDUCTORS

Figure 3 shows a cross section detailing a spring and its relation to the different underlying layers on a circuit wafer. The released springs are initially restrained by a load layer that prevents them from achieving their full unfettered lift geometry. The load layer is gradually relaxed during processing wherby the spring pairs controllably curl and interlock into each other to form coil windings.

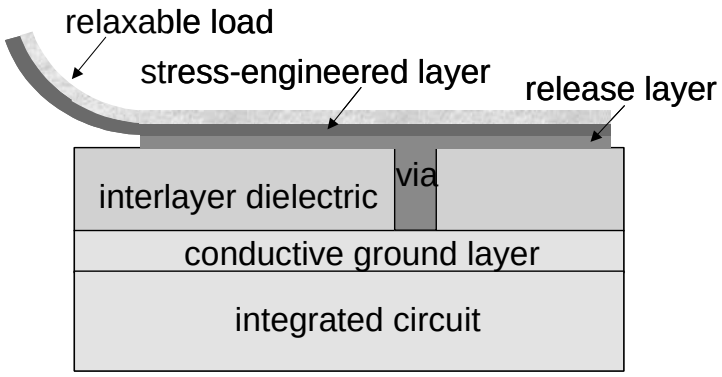

Figure 3: Cross section illustration of a released spring restrained by a relaxable load

Processing starts with the deposition of a Cu-plated metal layer on top of a silicon substrate. This ground plane layer serves as a current return path for the coil and is about 5 µm thick. The corresponding sheet resistance is about 5 mΩ/square. Our ground plane design allows eddy currents to run freely in the copper without causing significant resistive losses while shielding the silicon from the magnetic fields. A 12 to 15 µm-thick low-loss dielectric is spin-coated as a spacer layer to lower the coil's parasitic capacitance. Vias to the underlying metal layer are then opened.

A conductive release/sacrificial layer is sputter deposited next, followed by a thin layer of gold (Au), the stress-engineered MoCr film already described, and a final layer of Au passivation. This metal stack is about 1.5 µm thick and is deposited sequentially in a single pumpdown. An electrically conductive release layer is selected because it is also used as an electrode for electroplating the windings after coil assembly, as will be discussed. The stress-engineered film is a bi-layer with the first MoCr layer deposited at low pressure to achieve compressive stress; the second MoCr layer is deposited at a higher pressure to achieve tensile stress. The resulting built-in stress gradient produces a well-defined mechanical moment on the film.

The Au/MoCr/Au metal stack is patterned into individual springs that ultimately make up the coil windings. After defining the release masking windows, the springs are released from the substrate by undercut etching the sacrificial layer. The release mask is designed so that a piece of photoresist is retained on top of each spring after release. This resist material acts as a relaxable load that restrains the springs and prevents them from lifting fully during the release process. When heated, the load layer softens and gradually yields to the built-in stress moment in the spring metal, allowing spring pairs to move in a designed circular trajectory while gently and controllably self-assembling in air with high yield.

Figure 4 shows a self-assembled out-of-plane solenoid. The structure features an interlocking spring tip that provides a mechanical block which prevents paired springs from curling further after they come together. Once assembled, the devices are sufficiently robust for handling in and out of plating solutions without coming apart.

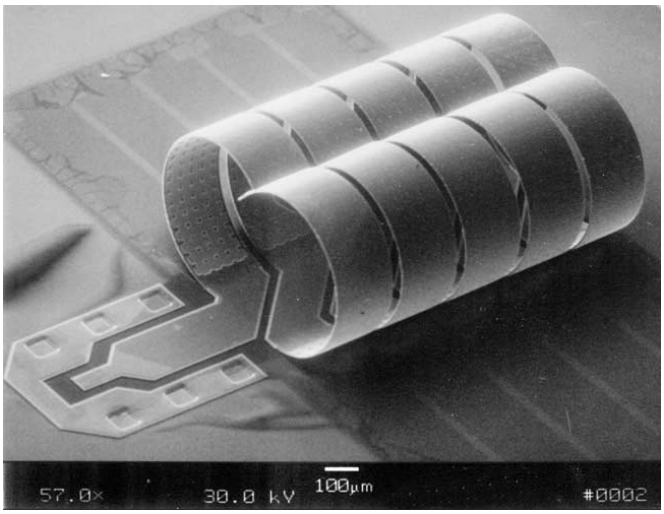

Figure 4: Self-assembled out-of-plane coil

The out-of-plane structure serves as a three-dimensional scaffold for copper plating. We electroplate a 5 to 8 µm thick copper skin on the scaffold to form low resistance coil windings. The gold layer in the spring metal stack works well as a plating seed. After release and assembly, all springs on the wafer are still electrically connected with each other through the conductive release material that remains in the non-released sections at the base of the springs and between the individual spring groups that make up a coil. In a plating bath, this remaining conductive release material provides a convenient common electrode for wafer-scale plating of the spring array. Also, the unreleased areas are still masked by a release window, preventing unwanted plating of the remaining release metal.

The copper plating not only fills the spring perforations but also electroforms the interlocked seam, joining paired springs into a solid and permanent connection. After plating, the release mask is removed and all remaining release material is cleared.

Our devices are designed for optimal operation at around 1 GHz – a frequency chosen for its relevance to wireless mobile communication applications. The coil traces are 200 µm wide on a pitch of 230 µm. The coil loop diameters are about 535 µm.

Since oscillator phase noise is the prime indicator for the in-circuit resonator Q^3, we built chips with balanced L-C oscillators around our out-of-plane coils alongside independent oscillators of identical circuit topology but with state-of-the-art spiral inductors. These chips were implemented in a commercial 0.6 µm BiCMOS silicon process. The spiral inductors were made out of the IC metals, and featured slotted poly ground planes for a peak Q of 8 to 10. Each oscillator was optimized to its specific inductor and designed to operate around 1 GHz with no attempt made to match their respective oscillation frequencies.

The out-of-plane coils were fabricated as described earlier, except on pre-processed BiCMOS circuit wafers instead of blank silicon wafers. The oscillator circuits used an earlier generation coil design with the return currents flowing through the IC top metal, rather than on a properly configured copper ground plane. The earlier generation coils have about half the Qs of our latest coils. Oscillators using the improved coil design with copper current return paths are being designed and processed.

We started again by depositing an interlayer dielectric on the wafer surface followed by opening vias to access the circuit contacts. The subsequent stressy metal release, self-assembly and plating steps were batch processed at the wafer scale. Figure 5 shows an array of finished MEMS coil oscillators prior to die singulation. Each die has MEMS coil oscillators placed side-by-side to spiral coil oscillators for comparison.

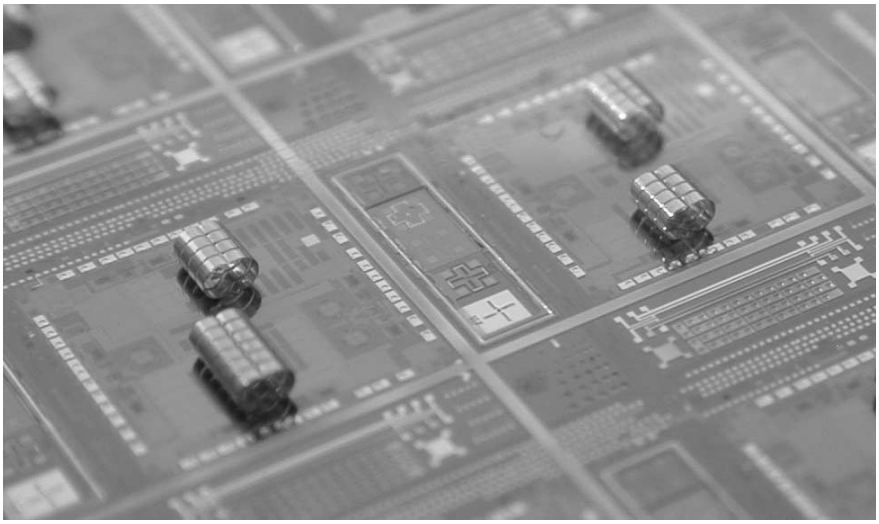

Figure 5: Oscillator circuits using out-of-plane micro-machined coils

The processed wafers were sawed into individual chips using standard wet dicing equipments. Singulated chips were die-attached onto prototype ceramic packages using conductive epoxy, and the contact pads were wirebonded to the package leads for testing. The package chip carrier cavity was then molded in a low loss-tangent encapsulation compound that completely embeds the substrate, coils, and wirebonds.

4. DEVICE CHARACTERISTICS

We characterized solenoids with different number of winding turns fabricated on 15 to 20 ohm-cm p-type silicon. The substrate is representative of the silicon wafers used in commercial CMOS and BiCMOS processes. The test pads of each microcoil sample were designed to match the ground-signal-ground terminals of the test probe (Figure 4). The signal pad connected to one coil terminal and the ground pads connected to the other terminal via the metal underneath the underspring dielectric.

We used the RF-IV technique[4] to get the best Q measurement accuracy over the frequency range of interest. The raw impedance data obtained were matched to that of an equivalent three-element coil model consisting of an inductor Ls in series with a loss resistor Rs, and a resonance capacitor Cs in parallel with the inductor and the resistor. The quality factor Qs was then taken as $Qs = \omega Ls/Rs$. This model de-embeds the coil properties from parasitic capacitances and yields an accurate expression for determining coil performance up to and slightly beyond the first resonance frequency.

Figure 6 shows measured inductances and quality factors. We obtained quality factors of 60 to 85 at 1 GHz., which are 8 to 10 times better than the best planar spiral coils on unaltered CMOS silicon. Moreover, these Q values are close to the theoretical maximum for our coil geometry assuming only skin effect losses in the windings.

Packaged oscillators were examined with a HP8561E spectrum analyzer equipped with a HP85671A phase noise utility. The MEMS circuits oscillated at 1.215 GHz with a phase noise of -110.9 dBc/Hz at 100 kHz offset compared to 966.6 MHz oscillation frequency with a phase noise of -98.6 dBc/Hz at 100kHz offset for the spiral coil oscillators. These numbers correspond to a raw phase noise improvement of 12.3 dB. The normalized phase noise

improvement is 14.6 dB when the frequency and power differences are factored in[3]. These results are consistent with our simulation models and direct coil measurements, and indicate a roughly four to five-fold improvement in Q factor – from 8 to 10 for the spiral coils to 35 to 40 for the MEMS coils. As mentioned earlier, the MEMS coils used in our oscillator circuits had lower Qs than our stand-alone coils due to differences in ground plane designs.

Finally, we verified that encapsulating the oscillator chips in molding compound does not degrade their phase noise characteristics – a result expected from direct coil measurements. The encapsulation experiments suggest that our devices are compatible with low cost injection molding IC packaging processes.

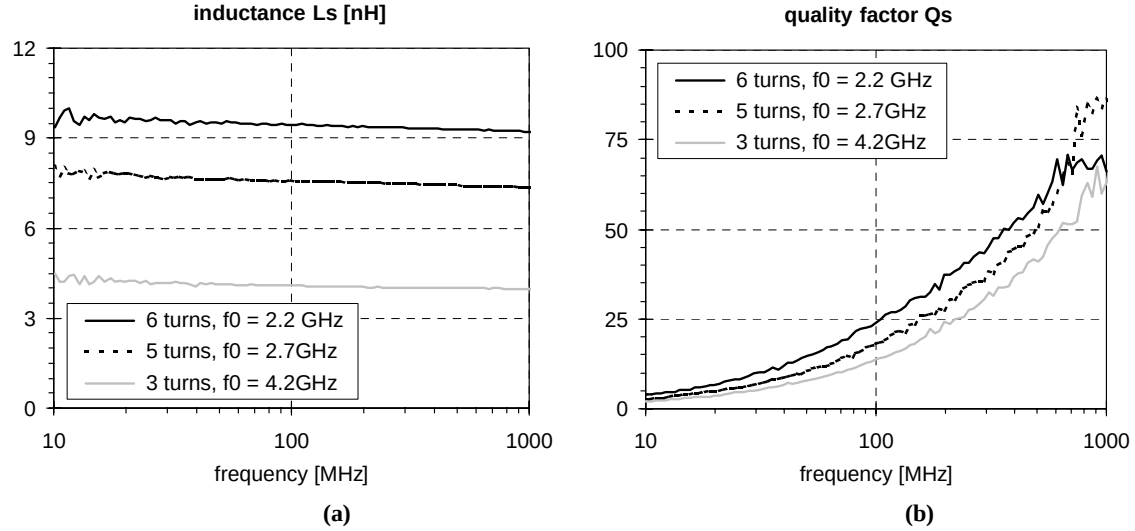

Figure 6: (a) Inductances and (b) Q-factors of out-of-plane coils with copper ground planes

5. SUMMARY

We present a novel out-of-plane inductor fabricated by three-dimensional self-assembly of stress-engineered films. The devices are made using simple batch processing techniques. The measured Q values of 60 to 85 at 1 GHz are among the highest reported for integrated coils on unaltered low-resistance silicon. We also achieved significant phase noise reduction in oscillator circuits utilizing these coils.

ACKNOWLEDGMENT

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