

A Digital Power Factor Correction using Floating Point Processor for Pulse Width Modulation Control in Boost Converters

¹Sanjay L Kurkute, ²Pradeep M Patil and ³K.C. Mohite

*¹Professor, Electronics Engineering Department, Bharati Vidyapeeth University
College of Engineering, Dhankawadi, Pune-43
Email : kurkutesanjay@yahoo.co.in*

*²Professor and Head, Electronics Engineering Department,
Vishwakarma Institute of Technology, Upper Indira Nagar, Pune-37
Email: patil_pm@rediffmail.com*

*³Professor, Physics Department, Officer on Special Duty, University of Pune, Pune
Email:kcmohite@gmail.com*

Abstract

This paper introduces novel digital and analog power factor correction techniques for single phase boost converter using pulse width modulation. It attempts to bring the input voltage waveform and input current waveform in phase with each other. In digital technique, switching is carried out using digital signal processor TMS320F2812. In analog technique, it is implemented using IC UC3854. In both these algorithms, the required duty cycles to achieve unity power factor are calculated and a boost converter is controlled by the pulses with pre-calculated duty cycles to achieve sinusoidal input current waveform. Also the input voltage feed-forward compensation network makes the output voltage insensitive to the input voltage and guarantees sinusoidal input current even if the input voltage is distorted. The said converter enhances a power factor correction from 49.80% to 98.40% for a load of 120 watts and 50.00% to 99.30% for a load of 400 watts.

Keywords: Power Factor Correction, Pulse Width Modulation, Digital Signal Processor, Boost Converter.

Introduction

The UC3854 provides active power factor correction for power systems that would otherwise draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion.

Digital implementation for power factor correction widely uses the average current mode control. The switching frequency in the conventional digital power factor correction control system is limited because of the sampling time delay and the necessary processing time. DSP controllers provide many distinctive advantages over traditional analog control, viz:

- Standard control hardware design for multiple platforms.
- Less susceptibility to aging and environmental variations.
- Better noise immunity.
- Ease of implementation of sophisticated control algorithms.
- Flexible design modifications to meet a specific customer need.

A predictive algorithm for digital power factor correction (PFC) is implemented and derived based on boost topology. All duty cycles required to achieve unity power factor in a half line period are generated in advance. A low cost DSP can be used to implement PFC operating at higher switching frequency. The power factor of 0.99 can be achieved under wide input voltage and output power conditions. The control strategy can achieve PFC for sinusoidal current waveform in transient state for step load change and input voltage change [1]. The theoretical aspects of PFC circuit, starting from basic principles and topological requirements having identified the ways in which simple dc to dc converters can be made to provide PFC is explained. The comparison of theoretical efficiencies of basic configurations, in which the power is processed that plays a crucial role in determining the overall efficiency of a PFC voltage regulator. This leads to the idea of a reduced-redundant-power-processing PFC voltage regulator [2]. The basic configuration of converters for achieving PFC and voltage regulation is explained in [3] based on a power flow consideration. Sixteen possible configurations are derived, from which PFC regulators can be constructed systematically. The overall efficiency can be improved if the power processed by one converter is not re-processed totally by the other converter within the PFC regulator. The stationary state equivalent circuit is used for PFC application in boost converter for one switching cycle. Analysis of the Buck converter with an LC input filter operating in discontinuous capacitor voltage mode and continuous inductor current mode that enables a very good understanding of the advantages and disadvantages offered by these operating modes. The analytical results represent a concrete design tool, which was not available previously. Fourth-order topology with galvanic isolation, operating in both modes explained and also analyzed [4]. The new alternating-edge-sampling algorithm is derived in [5] guaranteeing switching noise immunity. The average input current is used for control, it is important that the obtained samples accurately reflect the average input current. This allows accurate measure of the average input current. Discrete current mode control algorithm [6] that performs high power factor rectification for a boost converter, the controller input voltage sensing is not required, because of switching pulses get self-synchronized

with the frequency and phase of input voltage. Conventional phase locked loop is not needed as the controller works in stationary reference frame. Two decoupled fixed frequency current mode controllers generate the switching instants for the equivalent single phase boost rectifiers. Further these controls can be replaced by the latest technologies like neural in the literature [7- 8]. The work done for active power factor correction is in the literature [9-13].

Organization of the paper is as follows: Section-II describes the firing scheme using analog IC UC3854. Firing scheme using DSP ADMCF326 is explained in section III. Section IV shows the implementation of power circuit with variable load. The implemented results and discussions are stated in section V. At the end conclusions are stated.

Firing scheme using Analog IC UC3854

The integrated circuit UC3854 provides active power factor correction for power systems that would otherwise draw non-sinusoidal current from sinusoidal power lines. This IC implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. In order to achieve this, the IC UC3854 contains voltage amplifier, analog multiplier/divider, current amplifier, and fixed-frequency pulse width modulator. In addition to this, it contains a power MOSFET compatible gate driver, voltage reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator. UC3854 uses average current-mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients. The inbuilt high reference voltage and high oscillator amplitude minimize noise sensitivity while fast pulse width modulator elements permit chopping frequencies above 200 kHz. Thus UC3854 can be used in single and three phase systems with line voltages that vary from 75 volt to 275 volt and line frequencies of 50Hz to 400Hz range. The wonderful feature of UC3854 is its low starting supply current that reduces the burden on the circuitry that supplies power to this device. These devices are available in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

Fig 1 shows the block diagram of analog technique using IC UC3854. The power circuit of an analog technique comprises of a rectifier, an input inductor, a switching device, unidirectional diode, output capacitor and the load. In analog technique the power factor is improved by comparing the output voltage with a reference voltage which in turn is compared to the standard voltage generated by multiplying rectified voltage and the input current thereby improving the power factor by correcting the error and making input voltage and current in phase.

Fig 2 shows detailed circuit diagram of analog technique using IC UC3854.

Analysis of the power stage design in analog circuit makes use of a boost converter. The control circuit for a boost power factor corrector does not change much with the power level of the converter. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design

process is identical and the power stage is scalable, the corrector serves as model example and it can be readily scaled to higher or lower output levels.

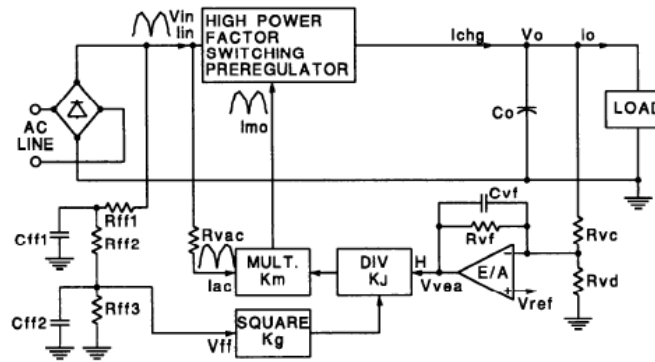


Figure 1: Block Diagram of Analog Technique.

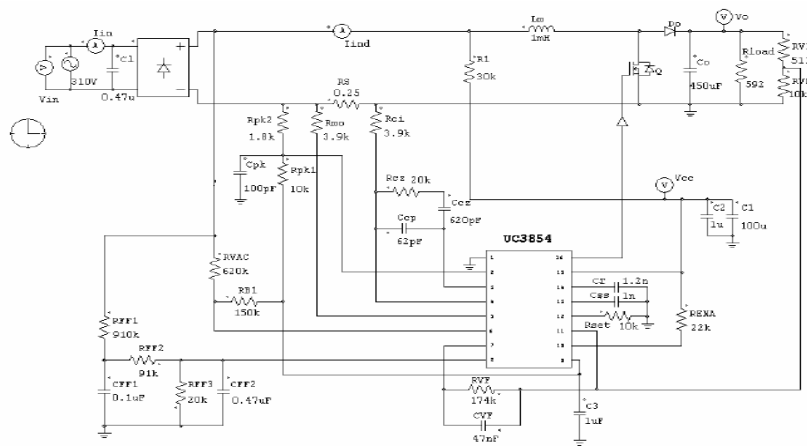


Figure 2: Circuit Diagram of PFC Using IC UC3854 (Analog Technique).

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and low enough to keep the efficiency high. In most applications, a switching frequency in the range of 20 KHz to 300 KHz proves to be an acceptable compromise. The value of the inductor would be reasonably small and cusp distortion minimized, the inductor would be physically small and the loss due to the output diode need not be excessive. Converters operating at higher power levels may find a lower switching frequency desirable to minimize the power losses.

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value

selection begins with the peak current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I_{line(pk)} = \left(\frac{\sqrt{2} \times P}{V_{in(min)}} \right) \quad (1)$$

where,

P is Input Power

The maximum ripple current in a boost converter occurs when the duty factor is 50% when the boost ratio $M = \frac{V_o}{V_{in}} = 2$. The peak value of inductor current generally does

not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. A larger value of ripple current will put the converter in the discontinuous conduction mode for a larger portion of the rectified line current cycle. This means that the input filter must be larger to attenuate more high frequency ripple current.

The value of the inductor L_m is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D_o at that input voltage and the switching frequency is given by,

$$L_m = \frac{V_{in} \times D}{f_s \times \Delta I} \quad (2)$$

where,

$$D_o = \frac{V_o - V_{in}}{V_{in}}$$

ΔI is Peak-to-Peak ripple current.

The factors involved in the selection of the output capacitor are the switching frequency, ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the *RMS* value of the switching frequency ripple current and the second harmonic of the line current.

The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise data. The hold-up time of the output often dominates other factors in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-

up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage at which the load will operate. Thus we define the capacitance value in terms of the holdup time.

$$C_o = \frac{2 \times P_{out} \times \Delta t}{V_o^2 - V_{o(min)}^2} \quad (3)$$

where,

C_o is the output capacitor

P_{out} is the load power

Δt is the hold-up time

V_o is the output voltage

$V_{o(min)}$ is the minimum voltage the load will operate.

The switch and diode must have ratings sufficient to insure reliable operation. The switch should have a current rating at least equal to the maximum peak current of the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have optimum level of derating depending on the application. The power MOSFET IRF460 has a 500V dc breakdown and 23A dc current rating has been selected as a switch. A major portion of the losses in the switch are due to the turn-off current in the high frequency switching diode MUR890. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the model circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation.

The average inductor current, is forced to follow the reference current, which is proportional to the rectified voltage, thereby reach unity power factor.

Firing scheme using DSP TMS320F2812

Fig 3 represents a block diagram for digital control strategy through which unity power factor is achieved. This strategy generates an error signal by which the output voltage remains constant in spite of load variations. With this strategy the phase difference between the input voltage and current has been minimized for achieving unity power factor.

The process in a digital controlled power factor correction is based on average current mode control that includes the following.

- Voltage and current sampling
- Voltage error calculation
- Voltage PI regulation
- Reference current calculation
- Current error calculation

- Current PI regulation and
- Duty cycle generation.

In digital implementation of average current mode control, the DSP or microprocessor is used to calculate the duty cycle in every switching cycle, based on the feedback and reference currents. The switch is controlled by the calculated duty cycles to achieve unity power factor. The system has an analog-to-digital converter to sample the output voltage, a computational unit to determine the value of the switch duty ratio, and a digital pulse-width modulator that outputs a pulsating waveform that controls the switch in the converter at the computed duty ratio.

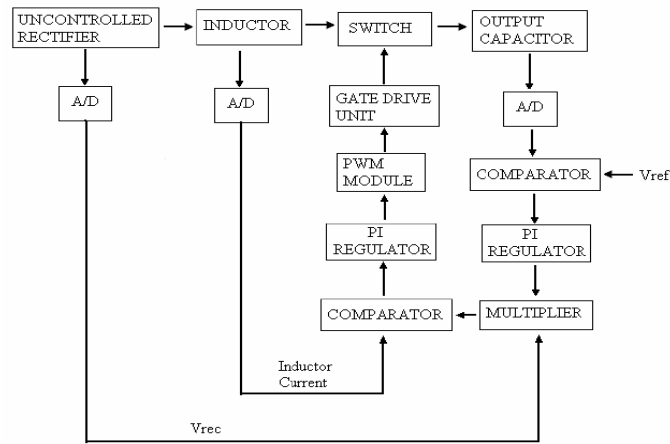


Figure 3: Block Diagram for Digital Control Strategy.

In the proposed method, TMS320F2812 is used for controlling PWM pulses. TMS320F2812 is a low cost, single chip DSP based controller. This DSP is code compatible with ADSP-21xx family. Thus instruction set of ADSP2181 processor can be used for programming. The features are

- (1) General purpose TMS320F2812 board.
- (2) Separate CPU and base boards for easy maintenance.
- (3) On board power supply, JTAG connector.
- (4) On board 16x2LCD module
- (5) Test points for important control signals.
- (6) 2812 General Purpose Board.
- (7) Compatible with the FLASH downloading software.

Fig 4 shows a schematic of interfacing power and control circuit. The circuit comprises of level shifter which shifts the level of the signal as DSP does not accept negative values. Also the gain of summing amplifier is adjusted in such a way that output of shifter stage (which is input to ADC) does not exceed 3.5V. The Op-Amp used in this circuit is IC 741 and the buffer IC7407 which drives the MOSFET.

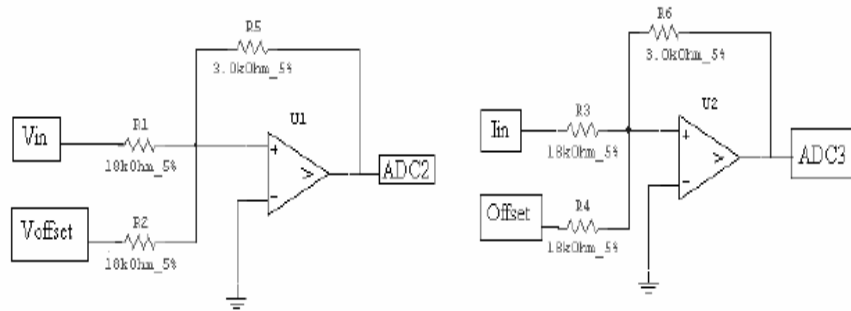


Figure 4: Interfacing Circuit for Digital Control Strategy.

Power Circuit

Fig 5 shows circuit diagram of PFC using digital technique wherein the output voltage is sampled and compared with the reference voltage. The error signal is input to the Proportional-Integrator (PI). The difference (or "error" signal) is then used to adjust some input to the process in order to bring the measured process value back to its desired set point. Unlike simpler controllers, the PI can adjust process outputs based on the history and rate of change of the error signal, which gives more accurate and stable control. PI controllers do not require advanced mathematics to design and can be easily adjusted (or "tuned") to the desired application, unlike more complicated control algorithms based on optimal control theory.

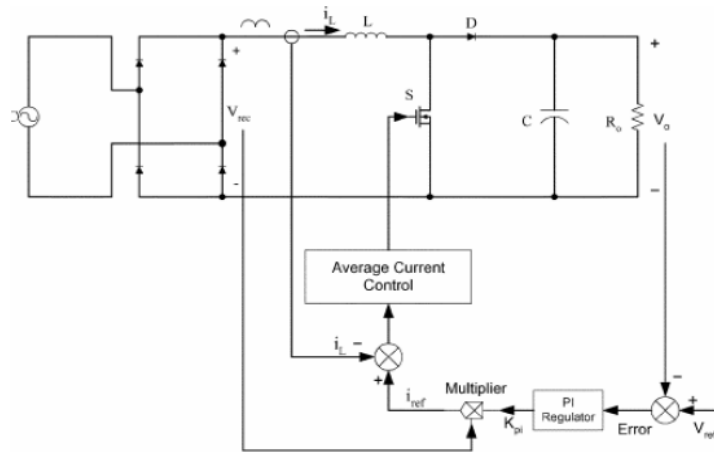


Figure 5: Circuit Diagram for Digital Control Strategy.

The PI output is fed to the Multiplier. Other input to Multiplier is the input voltage (rectified/mains). Multiplier generates the current reference. This reference current is then compared with the inductor current. The error is input to the PI regulator. The PI

output then controls the switching action of the MOSFET switch. Thus according to the fluctuations in output voltage the width of the PWM pulses would be varied in order to achieve PFC. Power circuit comprising of boost converter which generally consists of rectifier, input inductor, switching device MOSFET, unidirectional diode, output capacitor and load. In digital technique the power factor is improved by comparing the output voltage with a reference voltage, in turn compared with the standard voltage generated by multiplying rectified voltage and the input current. This improves the power factor by correcting the error and making input voltage and current in phase.

Results and Discussions

Table 1 shows the results carried out with the circuit, which is tested at various load conditions. It is observed that even though the load varies the output voltage remains constant and the power factor varies from 0.984 to 0.993.

Fig. 6.1 shows voltage and current waveforms without booster (without application of proposed PFC scheme) and Fig. 6.2 shows voltage and current waveforms with booster (with proposed PFC scheme) at the load of 120 Watt. It can be observed that the power factor improves from 48.80% to 98.40%. Fig. 6.3 shows voltage and current waveforms without booster and Fig. 6.4 shows voltage and current waveforms with booster at the load of 400 Watt. The power factor varies from 50.00% to 99.30%. Harmonic analysis is also carried out using power analyzer at load 400 Watt. Fig 7.1.shows the harmonic analysis, where fundamental component is observed as a dominant where as all other frequency components are suppressed.

Table 1: Results for implemented schemes for various load conditions.

Load		I/P Voltage (V)	I/P Current (A)	Voltage THD (%)	Current THD (%)	Voltage CF	Current CF	Output Voltage (V)	Output Current (A)	Power Factor (%)
120 W	without booster	196.2	1.00	1.50	176.3	1.41	3.62	388	0.309	49.80
	with booster	196.5	0.876	0.80	7.6	1.42	2.15	388	0.310	98.40
200 W	without booster	202.9	1.576	1.00	159.3	1.41	3.32	388	0.515	52.80
	with booster	201.5	1.376	0.70	6.7	1.43	1.66	388	0.518	98.90
400 W	without booster	191.0	1.56	1.40	139.2	1.40	3.09	388	1.030	50.00
	with booster	191.8	2.55	0.60	5.2	1.43	1.57	388	1.100	99.30

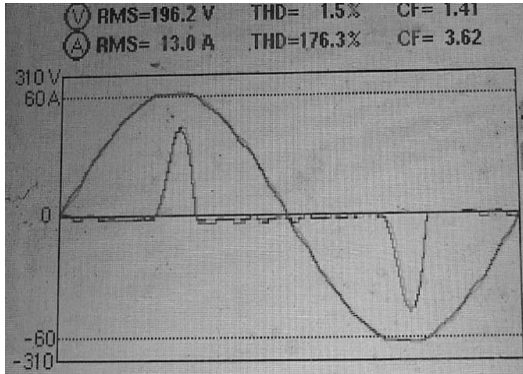


Figure 6.1: Without booster at load 120 watt.

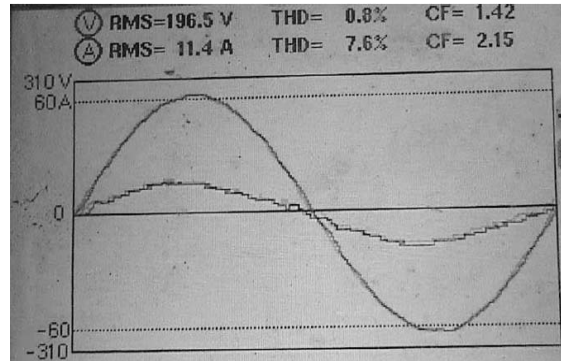


Figure 6.2: With booster at load 120 watt

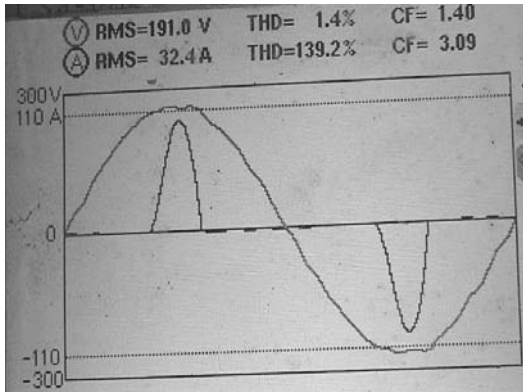


Figure 6.3: Without booster at load 400 watt.

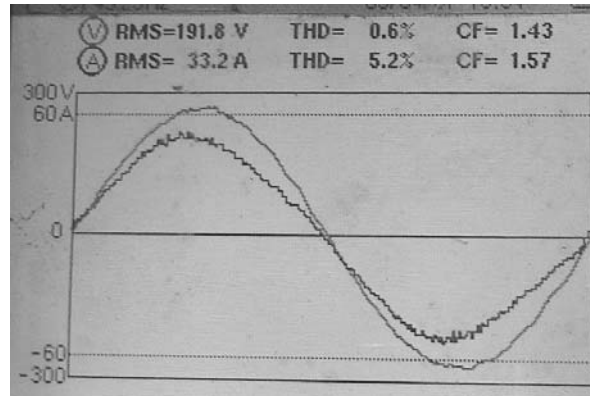


Figure 6.4: With booster at load 400 watt.

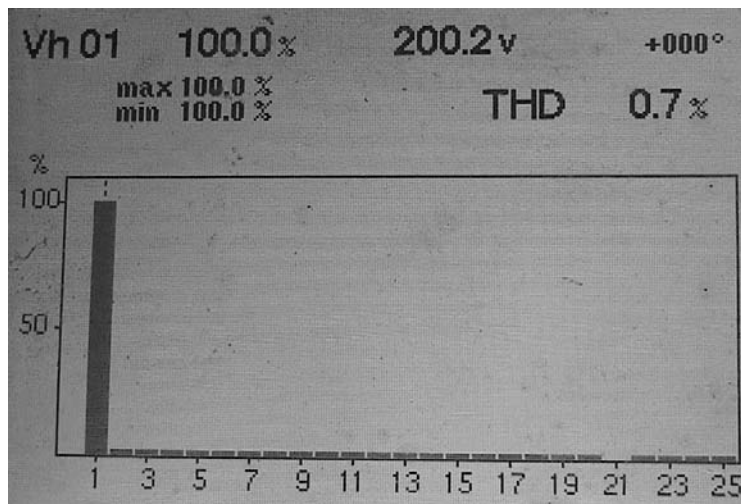


Figure 7.1: Harmonic Analysis with Load 400 W.

Conclusions

From the results obtained it is clear that the output voltage remains constant despite load variations and both input voltage and current are in phase. Power factor varies from 0.984 to 0.993 thus reducing the reactive power to a great extent. Advance Digital Signal Processors can be used in order to achieve higher frequencies. The power factor correction is applicable for Industrial variable speed drives, High Efficiency Servers, High efficiency Telecom AC-DC Converter, home appliances- Washing machines, Refrigerators, Compressors, Fans, etc where AC induction motors, Permanent magnet synchronous motors or Brushless DC motors are used. The control algorithm can be implemented by using FPGA will be the future scope of this work.

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