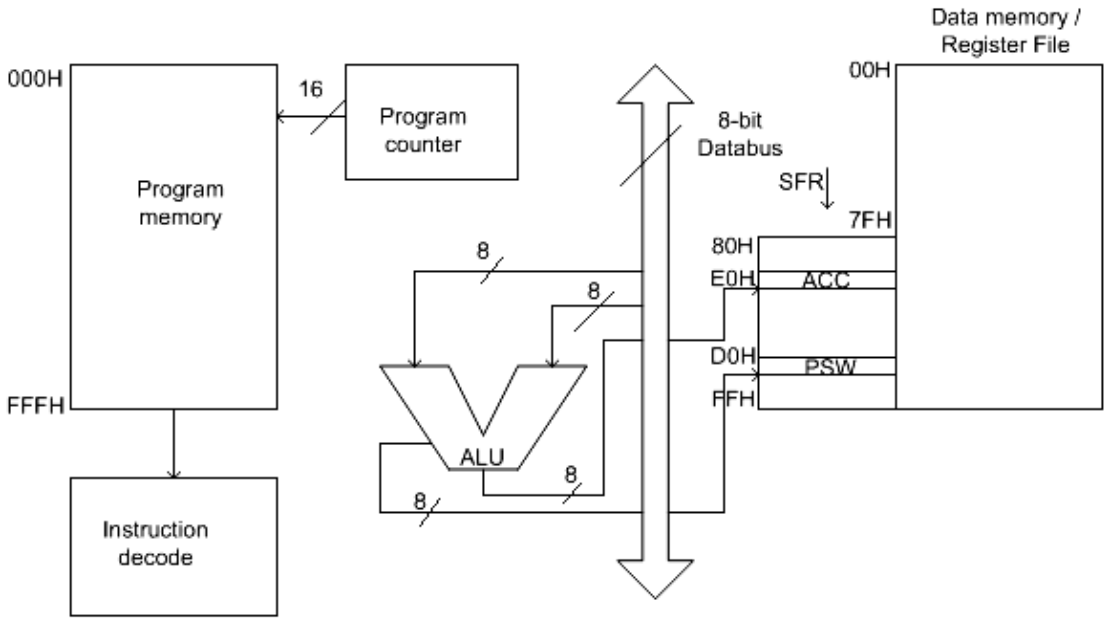
8051 PROCESSOR ARCHITECTURE



of registers is currently in use at any time when program is running. Register banks not selected can be used as general purpose RAM. Bank0 is selected by default on reset..

2. A bit addressable area of 16 bytes occupies RAM byte addresses 20h to 2fh, forming total of 128 bits. An addressable bit may be specified by its bit address of 00h to 7fh or 8 bits may form any byte address from 20h to 2fh.For example bit address 4fh is also bit 7 of byte address 29h. Addressable bits are useful when the program need only remember a binary event.
3. A general purpose RAM area above the bit area from 30h to 7f h, addressable as byte.

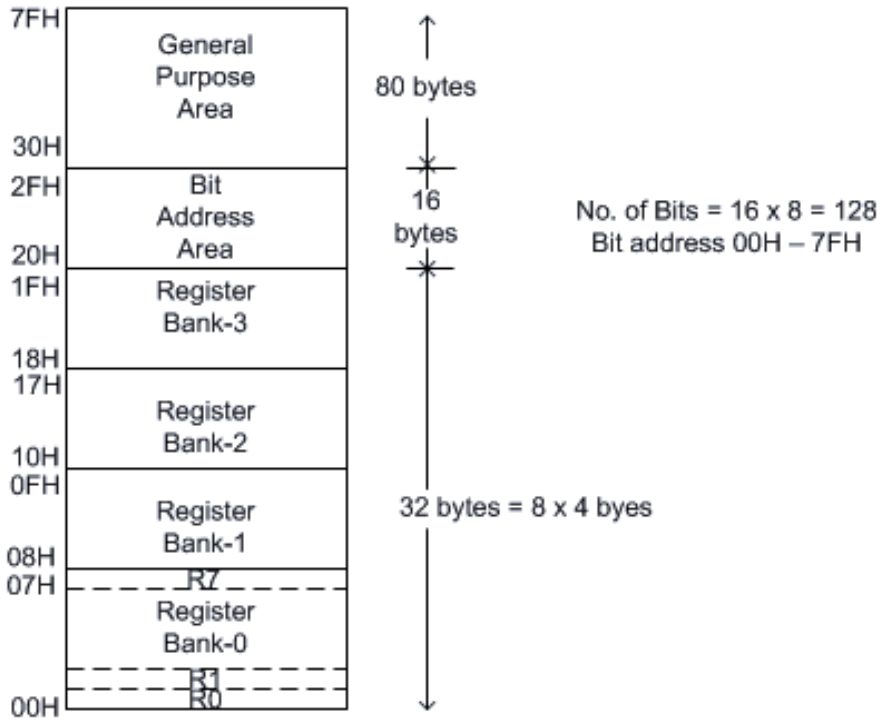


Fig.12. Internal RAM structure

The Stack and Stack pointer:

The stack refers to an area of internal RAM that is used in conjunction with certain opcodes to store and retrieve data quickly. The 8 bit Stack Pointer (SP) register is used by the 8051 to hold internal RAM address that is called the top of the stack. The address in SP register is the location in internal RAM where the last byte of the data was stored by stack operation.

When data is to be placed on the stack , the SP increments before storing data on the stack so that the stack grows up as data is stored. Whenever data is retrieved from the stack, the byte is read from the stack and then the SP decrements to point to the next available byte of stored data.

Operation of the Stack and Stack Pointer: Operation of the stack is shown in the above figure. The SP is set to 07 when the 8051 is reset and can be changed to any internal RAM address by the programmer. The stack is limited in height to the size of internal RAM. The stack can overwrite valuable data in register banks, bit addressable RAM and scratched pad RAM areas.It is programmer‘s responsibility to make it sure

that the stack does not grow beyond predefined bounds. The stack is normally placed high in the internal RAM by an appropriate choice of the number placed in SP register, to avoid conflict with registers or RAM.

Special Function Registers (SFRs):

The 8051 operations that do not use the internal RAM addresses from 00h to 7fh are done by a group of specific internal registers each called a specific function register (SFR) which may be addressed much like internal RAM using addresses from 80h to ffh.

Some SFRs are also bit addressable as is the case for the bit area of RAM. This feature allows the programmer the programmer to change only what needs to be altered leaving the remaining bits in that SFR unchanged. Not all of the addresses from 80h to ffh are used for SFRs . Only the addressed ones can be used in programming SFRs and equivalent internal RAM addresses are shown in Fig.10.
SFR Map: The set of Special Function Registers (SFRs) contain important registers such as Accumulator, Register B, I/O Port latch registers, Stack pointer, Data Pointer, Processor Status Word (PSW) and various control registers. Some of these registers are bit addressable (they are marked with a * in the Fig. 13 below). The detailed map of various registers is shown in the following figure.

The PC is not part of the SFR 0e0h or 8ch. and has no internal RAM address. SFRs are named in certain opcodes by their function names as A, TH0 and can also be referred by their addresses such as

Address

F8H								
F0H	B*							
E8H								
E0H	ACC*							
D8H								
D0H	PSW*							
C8H	(T2CON)*		(RCAP2L)	(RCAP2H)	(TL2)	(TH2)		
C0H								
B8H	IP*							
B0H	P3*							
A8H	IE*							
A0H	P2*							
98H	SCON*	SBUF						
90H	P1*							
88H	TCON*	TMOD	TL0	TL1	TH0	TH1		
80H	P0*	SP	DPL	DPH				PCON

Fig.13 Special Function Registers and the addresses

Internal ROM

8051 is organized so that data memory and program code memory can be two entirely different physical memory entities. Each has the same address ranges. The internal program ROM occupies code address space 000h to 0fffh. The PC is normally used to address program code bytes from address 0000h to ffffh. Program addresses higher than offfh which exceed the internal ROM capacity will cause the 8051 to automatically fetch code bytes from external memory, addresses 00h to ffffh by connecting the external access pin (EA) to ground.