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Reduction of Components in Cascaded Transformer Multilevel Inverter Using Two DC Sources

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Abstract – In this paper a novel cascaded transformer multilevel inverter is proposed. Each basic unit of the inverter includes two DC sources, single phase transformers and semiconductor switches. This inverter, which operates as symmetric and asymmetric, can output more number of voltage levels in the same number of the switching devices. Besides, the number of gate driving circuits is reduced, which leads to circuit size reduction and lower power consumption in the driving circuits. Moreover, several methods to determination of transformers turn ratio in proposed inverter are presented. Theoretical analysis, simulation results using MATLAB/SIMULINK and experimental results are provided to verify the operation of the suggested inverter.

Keywords: Determination of transformers turn ratio, Cascaded multilevel converter, Reduction of components

1. Introduction

Multilevel inverters are nowadays the preferredchoice for high-voltage and high-power applications inindustry. Recently, multilevel inverters have been widely applied in several industries such as motor drives, energy conversion, compensation device and etc [1-5].

In particular, multilevel inverters allow the operation at higher dc voltages using semiconductor switches connected in series and produce voltage waveforms with better harmonic profile than conventional two-level inverters.

There are several types of multilevel inverters; cascaded H-bridge [6-8], neutral-point-clamped, flying capacitor [9-11], and the others [12-14]. Particularly, cascaded H-bridge inverters have been focused inthese topologies because of the modularity and the simplicity [8]. Cascaded H-bridge inverters can also increase the number ofoutput voltage levels easily by increasing the number of H-bridges. However, if the number of output voltage levels isincreased, the number of switching devices is also increased,which makes a multilevel inverter more complicated. However, the cascaded H-bridge type multilevel inverter has a disadvantage that the independent DC-link voltage needs to be provided by each H-bridge separately. To reduce the number of independent DC sources, methods were introduced in recent years [15].

In this paper, a multilevel inverter using two DC voltage sources, single phase transformers and semiconductor switches is proposed. The number of switching devices and DC voltage sourcesof the proposed inverter is reduced. Capacitors, batteries, and other DC voltage sources can be usedas the voltage sources of the proposed inverter. Therefore, theproposed multilevel inverter can be applied to grid connected photovoltaic, fuel cell andetc systems. Proposed inverter can operates as symmetric or asymmetric converter.Single phase transformers are used in proposed topology therefore it can be used for high or medium voltage distribution system, as they require transformers to increase the inverter output voltage at the distribution level.

In section 2, the circuit topology of the proposed inverter is introduced. In section 3, the operation and application of the inverter is described. Simulation results are shown in section 4. In section 5the experimental results are shown.

2. Proposed multilevel Inverter

The cascaded H-bridge type multilevel inverter has a disadvantage that the independent DC-link voltage needs to be provided by each H-bridge separately. To reduce the number of independent DC sources the cascaded transformer inverter with two DC sources (CTITS) structure is proposed. In multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of voltage levels increases number of components and increasing the number of components increases the inverter circuit size, cost, installation area and control complexity. By the proposed circuit configuration, a number of switches and DC sources can be reduced. This topology has much significance for higher rated converters used for high or medium voltage distribution system, as they require transformers to increase the inverter output voltage at the desired level.

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Fig. 1 shows the circuit topology of the proposed inverter. This structure is made of two DC voltage sources and several single phase inverters.Fig. 2 shows the suggested basic unit for a single phase inverter.The basic unit shown in Fig. 2 can be cascaded as shown in Fig. 1.

Two DC voltage sources feed all basic units and are the same.The basic unit consists of a single phase transformer and three switches. Table 1 indicates the values of V_{o1} for states of switches S_1-S_3.The proposed multilevel converter requires unidirectional and bi-directional switches. The bi-directional switches with capability of blocking voltage and conducting current in both directions are needed in CTITS. There are several arrangement canbe used to create such a bi-directional switch. The common emitter anti-parallel IGBT with diode pair arrangement shown in Fig. 3 has been used in this paper. This bi-directional switch arrangement consists of two diodes and two IGBT.

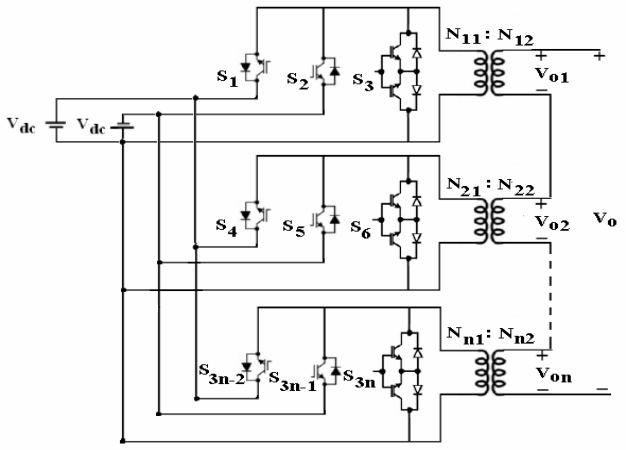


Fig. 1. Proposed cascaded topology.

In CTITS with *n* basic unit (or *n* transformer), always *n* switches must be turned on in different modes of converter operation but in conventional cascaded H-bridge multilevel inverters with n DC voltage source, number of on state switches is 2*n*. Imagine on-state voltage drop of one IGBT is considered V_D. We can talk on-state voltage drop of CTITS is lower than cascaded H-bridge multilevel inverters.

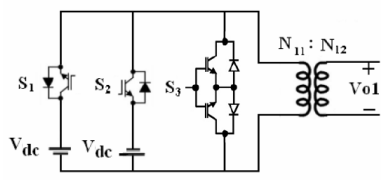


Fig. 2. Configuration of basic unit.

In CTITS, the number of switches is reduced and each switch requires one gate driver. Reduction of gate driver is obtained with reduction of switches number. One type of gate driver circuit has been shown in Fig. 3.

Table 1. V_{O1} for states of switchesin basic unit.

State	on switches	V_{O1}
1	S_3	0
2	S_1	$\frac{N_{12}}{N_{11}} V_{dc}$
3	S_2	$-\frac{N_{12}}{N_{11}} V_{dc}$

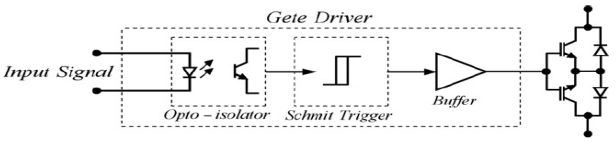


Fig. 3. Bi-directional switch and one type gate driver circuit.

Output phase voltage of proposedinverter is achieved by summing the output voltages of basic units. Output phase voltage is obtained by:

$$V_O = V_{O1} + V_{O2} + ... + V_{On} \quad (1)$$

The maximum output voltage (V_{Omax}) of cascade topology is:

$$V_{O\max} = \sum_{i=1}^{n} \frac{N_{i2}}{N_{i1}} V_{dc} \quad (2)$$

Operation of CTITS is the same as cascaded H-bridge multilevel inverters. In cascaded multilevel inverters, selection of DC sources magnitude is main part of inverter design but in CTITS, only two DC voltage sources exist and selection of turn's ratio of transformers is main part of design. By selecting proper switching functions, positive, negative, and zero voltages can be synthesized. The output voltages of basic units are cascaded through the secondary of the transformers. The input voltage to transformers is defined by switching functions of the basic units. Output voltage is sum of the transformers output voltages. The amplitude of the output voltage is determined by the input DC voltage source and turn ratio of the transformers. CTITS can operate in symmetric or asymmetric state to obtain uniform step voltage. To provide a large number of output steps without increasing the number of components, asymmetric multilevel converters can be used. In CTITS to obtain asymmetric multilevel converters turn ratio of transformers are selected in different value.Several strategies can be used for determination of transformers turn ratio in CTITS.

Number of components, voltage and current rating of semiconductor switches and on-state voltage drops of switches are basic problems that influence on volume, efficiency, control and cost in multilevel converters. Voltage and current ratings of the switches in a multilevel inverter affect on the cost and realization of the multilevel

inverter. Although volume and the number of components reduce in asymmetric cascaded H-bridge multilevel inverters but one of the important problems for asymmetric multilevel inverters is switches PIV. In the cascaded H-bridge multilevel inverters, the voltage standing on switches or PIV for switches is given by the following equation:

$$PIV_{sw,i} = V_i \tag{3}$$

$PIV_{SW,i}$ is switch PIV that put on in i th H-bridge cell and V_i is voltage sources of i th H-bridge cell. In symmetric cascaded H-bridge multilevel inverters, DC voltage sources of all H-bridge cells are the same ($V_i = V_{dc}$)so:

$$PIV_{sw} = V_{dc} \tag{4}$$

In asymmetric state, DC voltage sources of all H-bridge cells are not the same so switches PIV in different H-bridge cells are not the same and PIVs are affected by DC sources selection algorithms. In CTITS, a switch PIV in asymmetric state is the same as symmetric state.

In asymmetricmultilevel converters the number of switches is reduced and any level of voltage is produced with less number of switches, therefore voltage drop of asymmetric multilevel converters topologies is less than symmetric inverters.

2.1 Determination of transformers turn ratio in CTITS

In the following, we propose sixmethods for determination of transformers turn ratio for *n* cascaded basic units. Existence of different algorithm to determine transformers turn ratio gives freedom action to designer for design multilevel inverter.

In all method suppose that:

$$N_{i1} = p\ ,\ \ N_{12} = q\ ,\ \ i = 1,2,3,....,n \tag{5}$$

2.1.1 First method

If all turn ratios of transformers are the same, the inverter is known as symmetric multilevel inverter.The maximum number of phase voltage levels is given by:

$$m = 2n + 1 \tag{6}$$

n, m are the number of transformer(or basic units) and the maximum number of levels of phase voltage, respectively. The maximum output voltage (V_{Omax}) is:

$$V_{O\max} = n\frac{q}{p}V_{dc} \tag{7}$$

2.1.2 Second method

In the second algorithm to obtain uniform step AMC, the turn ratio of the transformers are proposed to be chosen according to a geometric progression with a factor of three or Trinary algorithm. InTrinary algorithm, the turn ratios of the transformers are chosen according to the following equations:

$$N_{i2} = 3^{i-1}q\ ,\ i = 2,3,....,n \tag{8}$$

Maximum number of output voltage levels is given by:

$$m = 3^n \tag{9}$$

V_{Omax} is:

$$V_{O\max} = \frac{(3^n - 1)}{2}\frac{q}{p}\mathrm{V_{dc}} \tag{10}$$

2.1.3. Third method

The third method for determination of the turn ratio of the transformers is in progression with a factor of two (Binary).

$$N_{i2} = 2^{i-1}q\ ,\ i = 2,3,....,n \tag{11}$$

Maximum number of output voltage levels and maximum output voltage are:

$$m = 2^{n+1} - 1 \tag{12}$$

$$V_{O\max} = (2^n - 1)\frac{q}{p}\mathrm{V_{dc}} \tag{13}$$

2.1.4 Fourth method

In the fourth method, the turn ratio of the transformers is suggested to be chosen according to the following equations:

$$N_{i2} = 2q\ ,\ i = 2,3,....,n \tag{14}$$

The maximum number of output voltage levels is given as:

$$m = 4n - 1 \tag{15}$$

Maximum output voltage is:

$$V_{O\max} = (2n - 1)\frac{q}{p}V_{dc} \tag{16}$$

2.1.5 Fifth method

In the fifth algorithm, the turn ratio of the transformers is chosen as bellow:

$$N_{22} = 2q\ ,\ N_{i2} = 7N_{(i-2)2}\ ,\ i = 3,4,....,n \tag{17}$$

The maximum number of output voltage levels can be determined as:

$$m = 7^{n/2}\ n \text{ is even} \tag{18}$$

$$m = \frac{(7^{(n+1)/2} - 1) + 2(7^{(n-1)/2} - 1) + 3}{3} \quad n \text{ is odd} \tag{19}$$

Maximum output voltage is:

$$V_{O\max} = \frac{(7^{n/2} - 1)}{2}\frac{q}{p}V_{dc} \qquad n \text{ is even} \tag{20}$$

$$V_{O\max} = \frac{(7^{(n+1)/2} - 1) + 2(7^{(n-1)/2} - 1)}{6}\frac{q}{p}V_{dc}\ n \text{ is odd} \tag{21}$$

2.1.6 Sixth method

In the sixth algorithm, the turn ratio of the transformers is given by following equation.

$$N_{22} = 3q\ ,\ N_{i2} = 7N_{(i-2)2}\ \ ,i = 3,4,....,n \tag{22}$$

The maximum number of output voltage levels and maximum output voltage can be calculated as:

$$m = \frac{4}{3}(7^{n/2} - 1) + 1 \qquad n \text{ is even} \tag{23}$$

$$m = \frac{(7^{(n+1)/2} - 1)}{3} + 7^{(n-1)/2} \quad n \text{ is odd} \tag{24}$$

$$V_{O\max} = \frac{4}{6}(7^{n/2} - 1)\frac{q}{p}V_{dc} \quad n \text{ is even} \tag{25}$$

$$V_{O\max} = (\frac{(7^{(n+1)/2} - 1)}{6} + \frac{7^{(n-1)/2} - 1}{2})\frac{q}{p}V_{dc}\ n \text{ is odd} \tag{26}$$

3. Operation of CTITS

Fig. 4 shows proposed topology with three basic units. The magnitude of each voltage source (V_{dc}) is considered 50 V. Here, turn ratio of transformers are selected according to first method (all turn ratio of transformers are the same). Operation of multilevel converters depends on the modulation methods. There are several modulation strategies for multilevel converters. Several modulation techniques have been proposed for cascaded multilevel inverters. Modulation techniques for cascaded multilevel inverters are usually an extension of the two level modulations [12-17].

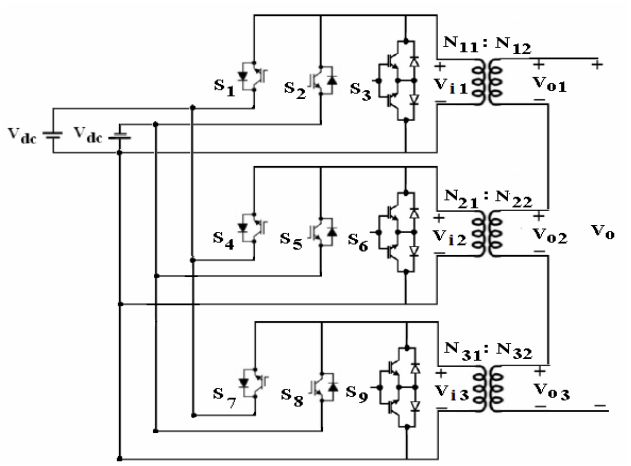


Fig. 4. Proposed topology with three basic units.

According to its switching frequency they can be classified as: fundamental switching and high switching frequency. According to high switching frequency different algorithm are introduced in recent years [16].

Among these methods, the most common used is the multi-carrier sub-harmonic pulse width modulation (MCSHPWM). The principle of the MCSHPWM method is based on a comparison of a sinusoidal reference waveform, with shifted carrier triangular (or DC) waveforms. Operation of 7-level CTITS has shown in Fig. 5. In the other hand, Fig. 5 shows relation between input signals of switches gate (switching) and output waveform of voltage. From comparison among sine wave and DC waves seven pulses are created. These pulses are used to switching with notice to lookup table of multilevel switching. Lookup table of 7-level CTITS is shown in table 1. For example if sine wave greater than second carrier and lower than third carrier then P2 is created and this pulse for production of second level is given to S_1, S_4 and S_9. In Fig. 5(b), Z indicates to zero level, P1, P2and P3 indicate to positive levels and N1, N2and N3 indicate to negative levels. Fig. 5(c) shows gate signals of switches. Output voltage is shown in Fig. 5(d).

Table 1. Look up table of switching.

Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$+3V_{dc}$	on	off	off	on	off	off	on	off	off
$+2\ V_{dc}$	on	off	off	on	off	off	off	off	on
$+\ V_{dc}$	on	off	off	off	off	on	off	off	on
0	off	off	on	off	off	on	off	off	on
$-\ V_{dc}$	off	on	off	off	off	on	off	off	on
$-2\ V_{dc}$	off	on	off	off	on	off	off	off	on
$-3\ V_{dc}$	off	on	off	off	on	off	off	on	off

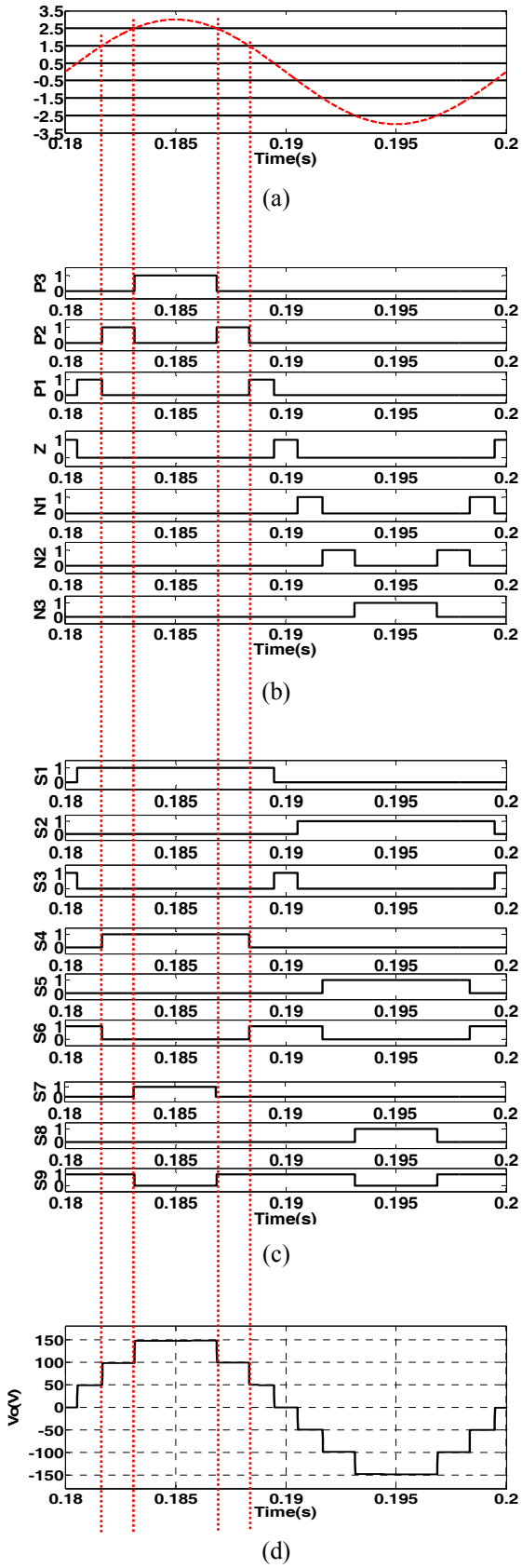


Fig. 5. Operation of 7-level CTITS: (a) modulation waveforms; (b) switching pulses; (c) gates signals; (d) output phase voltage.

3. Simulation results

Several strategies can be used for determination of transformers turn-ratio in CTITS. In the previous section operation of symmetric CTITS has been shown. To evaluate the expected performance of the CTITS in the generation of a desired output voltage waveform, a prototype is simulatedbased on the proposed topology according to that one shown in Fig. 4. The simulation results carried out by MATLAB/SIMULINK. Here among determination transformers turn-ratio methods, second method is selected.If the turn-ratio of transformers is chosen as 1:1, 1:3 and 1:9, this circuit can generate twenty seven level voltages. In this simulation, V_{dc}=1 pu and output frequency is 50Hz.

The output voltages of single phase transformers are shown in Fig. 6(a), 6(b) and 6(c). Output phase voltage of CTITSinverter is achieved by summing the output voltages of basic units.The output voltage waveform and harmonic spectrum of output voltage are shown in Fig. 7(a) and 7(b), respectively. The CTITS has twenty seven-level voltages per phase with the fewest components. Total harmonic distortion (THD) of output voltage is as low as 5%. It can be observed from the harmonic spectrum of voltages that, presented topology is effective to meet low harmonic level.

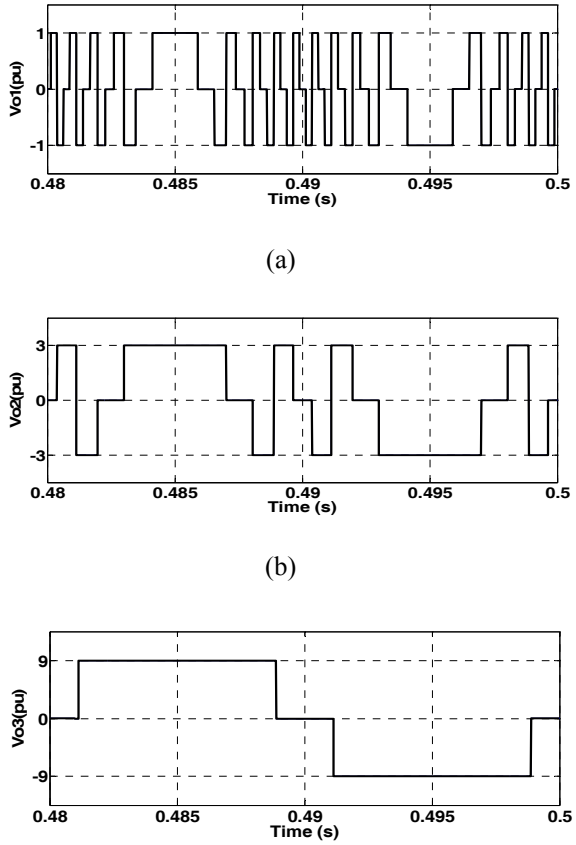
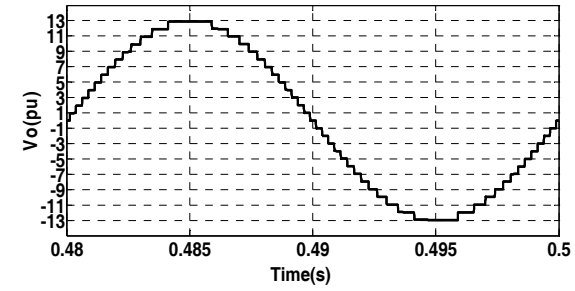
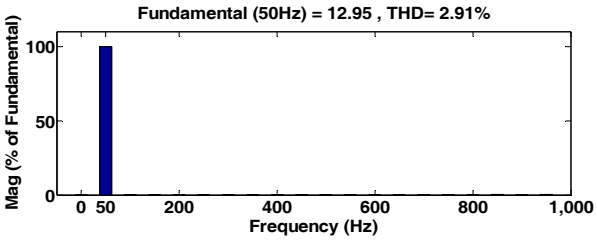


Fig. 6. Output voltage of inverter modules.



(a)



(b)

Fig. 7. (a) Output voltage; (b) harmonic spectrum of output voltage.

4. Experimental results

To verify the performance of the proposed inverter experimentally, a prototype has been built in the laboratory scale.In order to validate the proposed concept, the inverter of Fig. 4 was constructed and tested in the 27-level mode.

To get 27 output voltage levels of the inverter, the ratio of transformers is arranged as second method (Trinary). The turn ratios of the transformers are set to 12:12, 12:36 and 12:108. The DC sourceswere supplied by two battery sources that they have a voltage of 10V. This multilevel generates staircase waveform with maximum 130 V and 50 Hz in no load state. The common MOSFET with internal anti-parallel diodes has been used in prototype. The bi-directional switch arrangement consists of two diodes and two MOSFETs. The MOSFETs are the types IRFP460 with voltage and current ratings equal to 500V and 10 A, respectively. The ATMEGA32-8PT microcontroller by ATMELL company has been used to generate the switching patterns and the opto coupler TLP521-1 is used to drive switches. Fig. 8 shows the photo of experimental prototype of proposed inverter.

Fig. 9 shows the output voltage of different inverter modules in no load state. As shown in Fig. 9 the input voltage of each inverter has negative, positive or zero values and there is not any problem about transformer saturation. Fig. 10 shows the output voltage of proposed inverter.

As it can be seen, the results verify the ability of CTITS in generation of desired output voltage.When the load is a series R–L with resistance 130 Ω and inductance(90 mH,

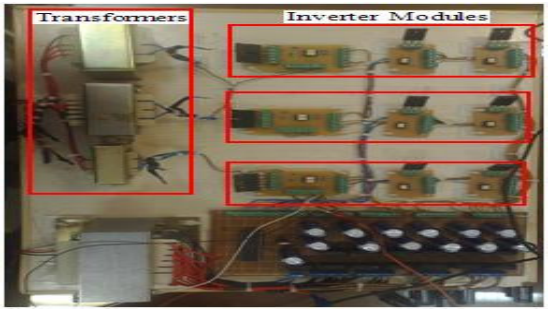
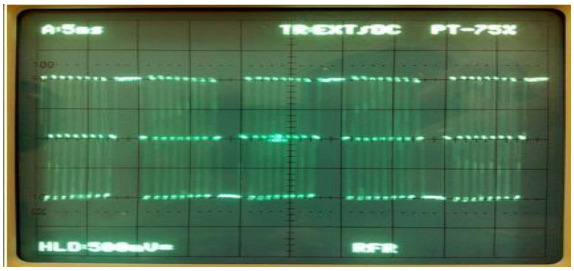
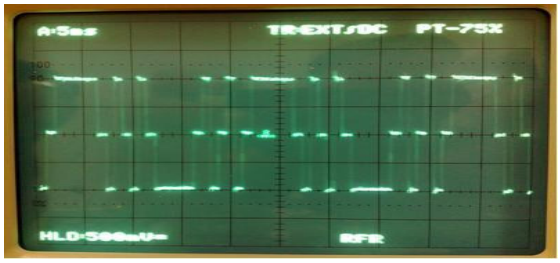


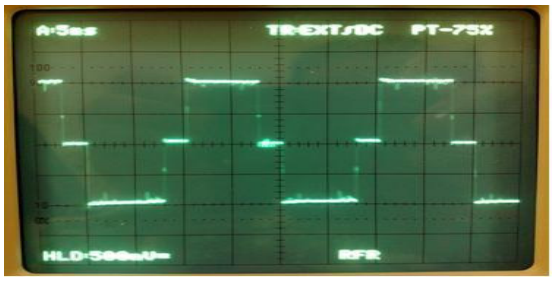
Fig. 8. The prototype.



(a)



(b)



(c)

Fig. 9. Output voltage of inverter modules, 0.5*10 volt/div.

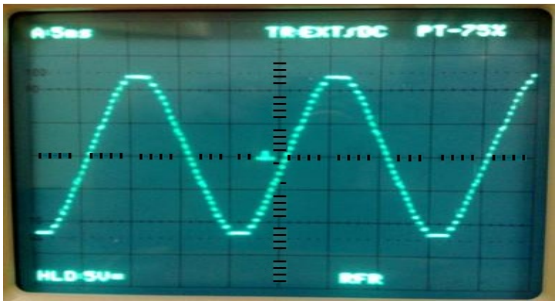


Fig. 10. The output voltage, 5*10 volt/div

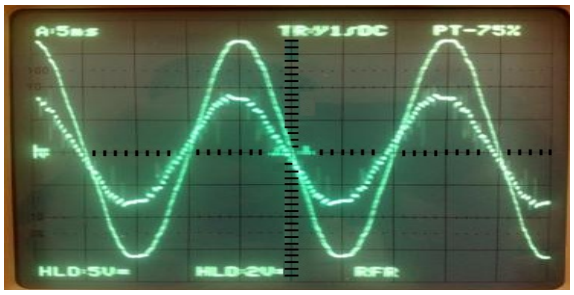


Fig. 11. Measured output voltage, 5*10 volt/divand load resistant voltage(current), 2*10 volt/div

25 Ω), respectively measured output voltage and resistant voltage (current) have been shown in Fig. 11. The voltage magnitude of DC sources is equal to 7 V.With three basic units per phase, however, symmetric CTITS generates only 7 voltage levels that is shown in previous sectionand a Tinary CTITS generates 27-levels in each phase. The more output voltage levels in multilevel inverters caused, the more nearly a sinusoidal waveform can be synthesized. Thereby, with the Trinary topology, total harmonic distortion (THD) can be reduced greatly.

5. Conclusions

This paper proposed a cascaded multilevel inverter employing low-frequency single-phase transformers and two DC input power source. The proposed circuit configuration can reduce a number of switches and DC sources compared with conventional cascaded H-bridge multilevel inverters. Six methods for determination of transformers turn ratio for *n* cascaded basic units have been introduced in this paper. This object gives freedom action to designer for design multilevel inverter.The performance of the proposed multilevel inverter has been verified by simulation and measurement results.

Acknowledgment

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