Printed circuit boards-Selecting a board finish

Introduction

So far in this course we have looked at the materials of which the inner sections of the board are made, and at the components that will be assembled on it. Now it is time to look in a little more detail at the materials and processes involved in creating a surface to which components can be attached reliably and at high yield.

Inevitably we will be looking both at mainstream processes and other finishes which have advantages for certain applications. The two front runners are Hot Air Solder Levelling (HASL) and Electroless Nickel Immersion Gold (ENIG): both have a long history, and many adherents. However, there are quality and environmental issues affecting both finishes, and a great deal of attention is currently being paid to this topic. By the end of this Unit, you should have a good understanding of:

why the existing finishes are favoured

the design and process implications of their use

which processes are being evaluated as alternatives.

Requirements

Like yours, our lists are probably not exhaustive, but we have tried to structure them in terms of three different perspectives, those of somebody who makes the board, somebody who is trying to assemble components on to it, and your perspective, as a designer anxious to provide the right finish for the right application, within constraints of cost and feasibility.

A fabricator is primarily interested in being able to carry out a process cost-effectively and safely, so his “wish list” would concentrate on issues of cost and ease of process control.

An assembler is primarily interested in getting a good first-pass yield, so his wish list concentrates on whether the board will produce high yields with the process he is running.

From a designer’s point of view, the key is that the finish should be compatible with his application:

Each application will have different requirements for surface flatness and definition

There are special requirements for wire bonding and for the use of the board finish to make a switch contact or connector

The ability of the surface finish to withstand multiple heat cycles will influence the range of available options – for example, material which deteriorates after the first reflow soldering cycle may be totally unsuited to requirements with double-sided surface mount assembly and expect a high amount of rework

A designer will also take into account the reliability of the assembly under adverse environmental conditions

The range of suitable board finishes will depend on the end user specification.

Table 1: Different perspectives on the requirements for a board finish

Fabricator	Assembler	Design
cost	shelf life	surface flatness
ease of process control	handling	definition
waste issues	cost	range of applications (fine pitch SMT; BGA and µBGA; flip chip; wire bonding; contact; connector; high reliability)
safety	flux compatibility	withstands multiple heat cycles
	solderability	passes SIR/environmental requirements

Before looking at different materials, we are going to examine in a little more detail some of the elements within this list of issues.

Surface flatness

Your experience, and observation of a range of boards, will probably have indicated that a HASL surface is generally used, except for those applications where the designer has used fine pitch devices, BGAs, and other high-density components.

You may also have realised from observation that the HASL surface is not very flat, its deviation from flatness depending partly on the pad design, and partly on the board vendor. In fact, flatness is an issue which occurs both in relation to the flatness of the board as a whole, an issue that we will return to in Aspects of board quality, and the flatness of the pads on its surface. The requirement is two-fold:

In the first instance, the leads of any component have to make contact with the solder paste in order for joints to be formed. Because slight pressure is applied to a component during placement, we normally allow the lead to depress the paste only to around half its original height, in order to reduce possible bridging, this means that the surface on the area of the component has to be flat within half the paste height, that is typically 75µm

The component lead has to be in contact with sufficient solder to enable the joint created to have the right volume. As you will realise, joints which are “insufficient” have reduced reliability.

One further consideration is that the pads themselves should be sufficiently flat to avoid components placed on them skidding off during placement.

So we are looking for flatness and evenness of coating, and the requirements get more difficult to achieve with fine pitch components and with area devices such as BGAs and micro BGAs.

Solderability

If you have ever carried out any soldering, or been involved in fault-finding, you will appreciate that problems associated with soldering may derive from the quality of the surfaces to be soldered, from the soldering technique and, in the case of hand soldering, from the ability and training of the operator!

For the assembly industry as a whole, however, many of the common problems associated with soldering can be traced back to poor solderability. The trend towards materials with mild fluxing activity has accentuated the problem.

Imagine that you are an assembly house experiencing problems in assembling a circuit. You get poor yield, or a lot of rework, or find that you have to adjust the process to get good results. You suspect that the problem is to do with solderability, either of the board or the components. How do you set about finding where the problem lies, with the supplies you buy in, with your materials, or with your process?

Before we look at how solderability might be assessed, we are going to have a quick review of the requirements for soldering.

Removing the oxide coat

Even with the most solderable metals, some cleaning of the surfaces to be soldered is needed. This is because most metals show a strong tendency to form compounds with oxygen from the atmosphere and are rapidly covered with an oxide film when exposed to the air, even at room temperature. On tin and copper, an oxide layer about 2nm thick is formed almost instantaneously. These oxides are generally removed by fluxes, which are capable of reacting chemically and physically with the oxides, and of dissolving or dispersing the reaction products.

Fluxes are applied before or during soldering and cover both the base metal and the solder. This retards oxidation by oxygen from the atmosphere, which would otherwise occur even more strongly at soldering temperature. In areas where the oxide film has been removed, a direct metallic contact is established between solder

and base metal, so that one single interface with low energy exists instead of the original two interfaces. From this point of contact the solder will spread.

Note that, if one works at too low a temperature, an oxide layer may still be present between the base metal and the solder. [Joints of this type are often called "cold joints", although the term is sometimes criticised – in fact defective joints can be produced by diffusion processes caused by excessive exposure to temperature, although the interface may then be an intermetallic rather than an oxide layer.]

For all such defective joints, the initial resistivity will be higher than for a good joint, but not necessarily unacceptable. However, the joint resistance is likely to increase the life, and the joint may become electrically noisy or even intermittently open-circuit. Adhesion is also poor, and the solder can easily loosen when subjected to a mechanical load.

Surface wettability

In order for a joint to be made, the solder needs to wet the conductive surfaces on the board and the component within the process time available. There are two measures of surface wettability which impact on the ability of component and board metallisation to make a satisfactory joint:

degree of wetting: how far the solder spreads

rate of wetting: how fast the solder wets and spreads

Related to these, and often tested at the same time, is the capacity of the metallisation to withstand exposure to molten solder without dewetting. Such tests are related to the 'process window' shown in Figure 1. This indicates diagrammatically the way in which a surface is first wetted by solder, and then at a later stage dewetted.

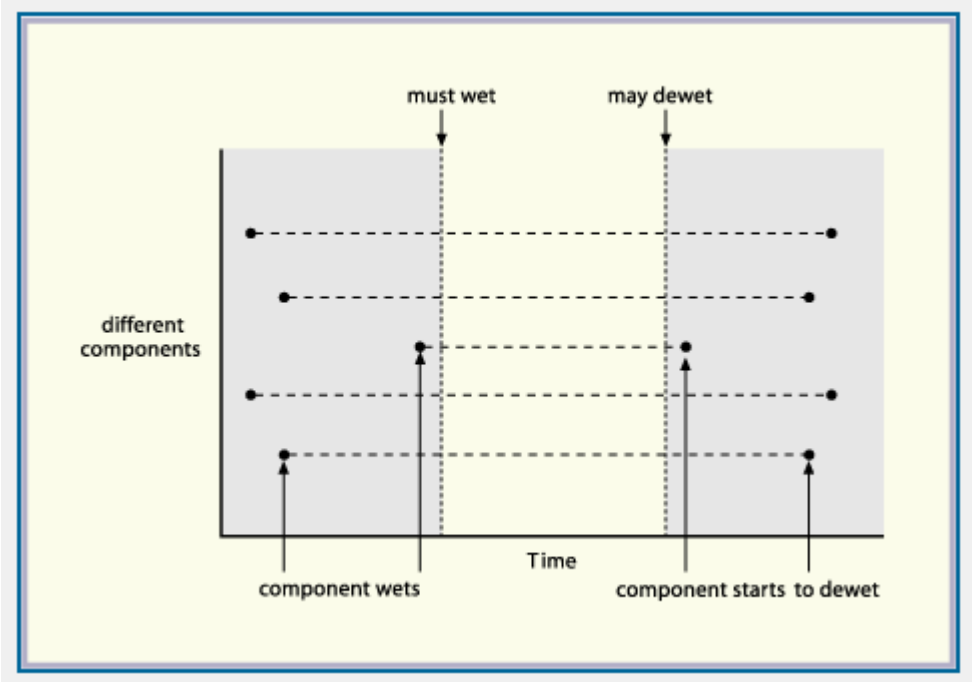


Figure 1: A process window for soldering

Note that different components show different characteristics; some wet quickly, others take a long time to wet. Similarly, some components are resistant to dewetting (take a long time to do this) whereas others dewet quickly.

Typically those components which wet quickly take a long time to dewet, whereas those that wet poorly dewet first. The process window is between the time when a component must wet (given the soldering conditions obtaining) and the first occasion on which components may dewet.

Solderability testing

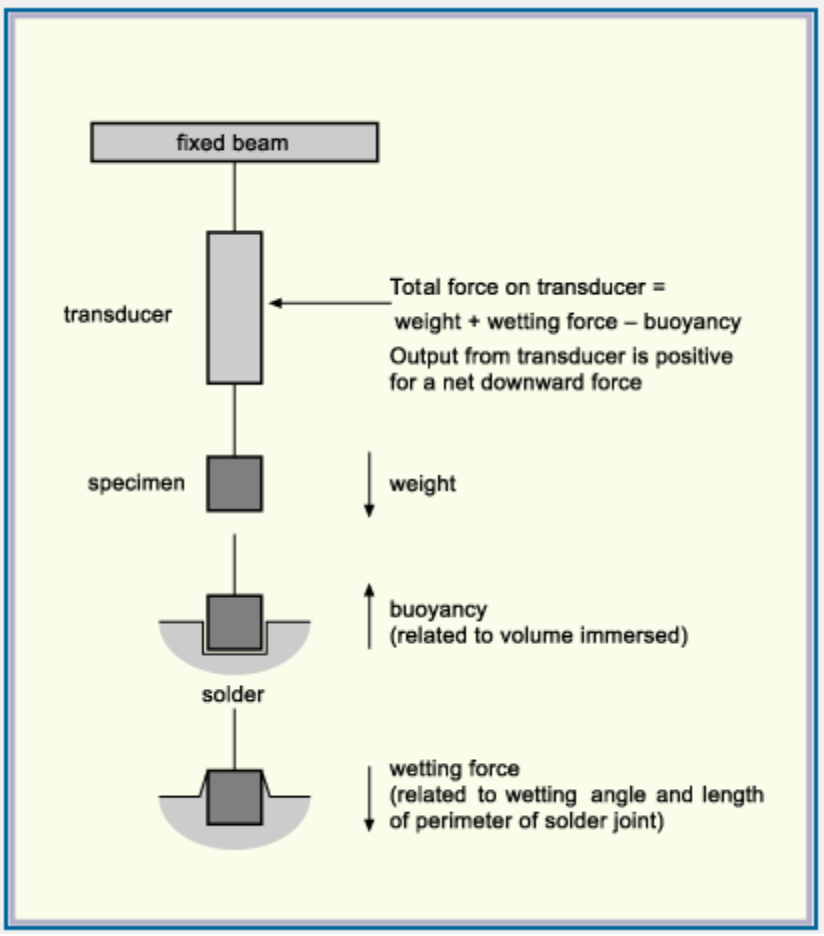
The idea of the process window helps us to explain our observations, particularly in terms of dewetting, but the assessment of solderability goes back to the basic ideas of "how far and how fast". However, it is just these fundamental measures which are difficult to carry out in production, except one might take a copper coupon with a bead of solder, and watch it spread.

In assembly shops the wettability of individual parts is most likely to be estimated using production equipment and observation. Whilst this helps answer the question "Will the parts work?", such tests are difficult to replicate and are not suitable as standardised assessments. Standardised tests need to have as few variable parameters as possible, and specify tight control of these.

Of the standardised tests available, the wetting balance test method has for long been regarded as the most versatile, and has been used for assessing the efficacy of fluxes as well as the solderability of components. Examination of the results gives information about both the speed and extent of wetting and the behaviour of the surface upon prolonged exposure.

The specimen is fluxed, then suspended from a sensitive balance and held over a solder bath which preheats it by convection. It is then immersed in the bath at a controlled rate and to a set depth. The specimen experiences vertical forces of buoyancy upwards and the surface tension downwards, which are detected by a transducer (Figure 2). The transducer output varies with time and is continuously recorded on a high-speed chart recorder or data acquisition computer: the forces change very rapidly and a fast response time is essential to avoid distorting the test results.

Figure 2: Forces on the transducer, explaining the positive and negative sense of the forces



In Figure 3, the six stages of the testing of a readily wettable specimen are shown:

just before immersion.

immediately after immersion, before wetting has begun and both buoyancy and surface tension forces act upwards.

after wetting has begun and the meniscus has risen up the specimen to the point where the vertical force from surface tension is zero and the net force acting in the specimen is that due to its buoyancy.

when the meniscus is curved upwards and the surface tension force is acting downwards.

as the specimen is being withdrawn and surface tension and a possible oxide film on the solder are causing solder to be dragged out.

when the specimen has been withdrawn and is heavier than at the start of the test because of the adherent solder coating.

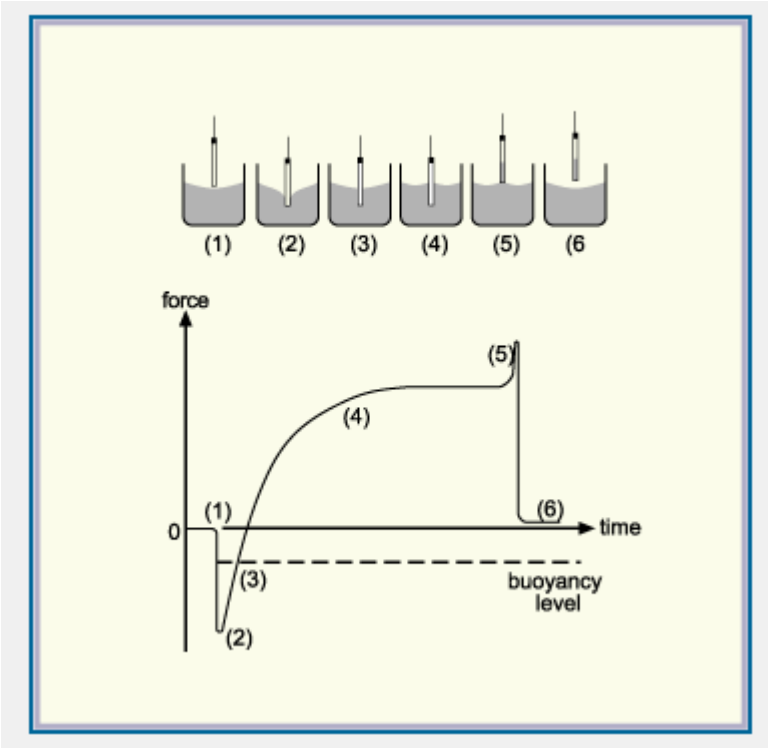


Figure 3: A wetting balance curve

Some representative curves are also shown in Figure 4. In each case the full horizontal line represents the force at the start of the cycle and the dotted horizontal line the buoyancy level at which the wetting force is zero (a calculation based on the weight of solder displaced).

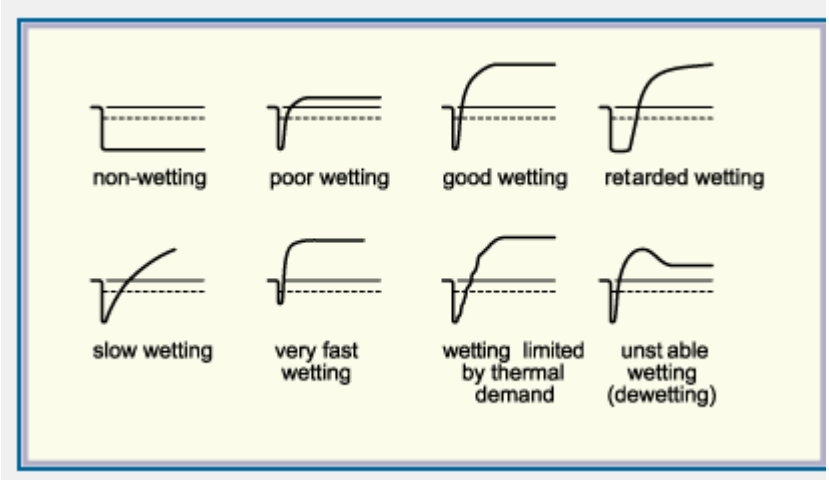


Figure 4: Representative shapes of wetting balance curves

In the globule balance normally used for SM components, the solder bath is replaced by a small globule of molten solder (Figure 5).

Figure 5: Wetting balance of the globule variety

There are several benefits:

individual leads or pads can be assessed separately

the curved solder surface increases the transducer output signal

the small globule reacts to effects such as dissolution of solderable coatings and metallisation which could be swamped in a large bath

new, uncontaminated solder can be used for each test.

Ceramic plate test

Not everyone accepts that the wetting balance test is suited for determining the solderability of plating materials. The ceramic plate test (CPT), developed at Compaq in 1988, is claimed to evaluate devices under conditions more closely simulating actual surface mount processing. The method consists of printing solder paste onto a ceramic substrate, followed by package placement and reflow. The reflowed solder on the leads is then inspected visually to determine the wetting characteristics, using a rating system for solder appearance (0=best; 10= worst).

Although this test is not universally accepted, the most important point to make is that the test results obtained with the ceramic plate test are not mirrored by the wetting balance test results, tending to be less favourable.

SERA

Solderability testing should ideally reflect the solderability of the surface after typical life. Unfortunately, board fabricators need to have immediate assessments, and other test methods have been proposed to try and give a more real-time test. One of these is Selective Electrochemical Reduction Analysis (SERA), which can be applied to assess the chemical constitution of the through-holes as well as the surface features.

Two test approaches are required to get a complete picture of the finish. The first is a non destructive reduction test which assesses the presence and quantity of surface oxides of tin. The second uses a destructive oxidation test where the electrolyte strips selectively through the layers of tin and the underlying intermetallics. Measuring the amount of free surface tin gives an indication of solderability. Whilst this test is under evaluation, and an interesting laboratory tool, the concern is that it may not be a good predictor of long-term solderability because the growth rates of intermetallic vary with the different types of tin finish.

Changes in solderability with time

Component solderability is extremely variable, depending on the type of material and the conditions in which it has been manufactured and stored. Damp and heat combined will do much to reduce the wettability of even the more robust surface. The solderability of components and boards can be assessed by a number of methods, the most reproducible of which is the wetting balance.

The deterioration with time of the solderability of a tin-lead coated surface is shown schematically in Figure 6.

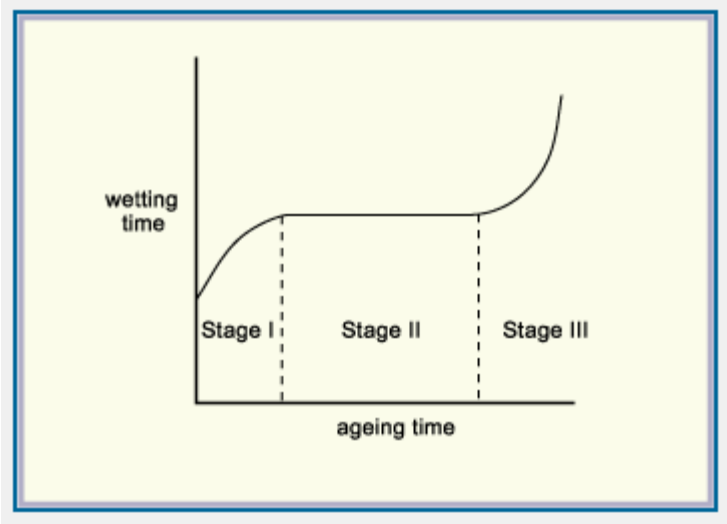


Figure 6: Schematic diagram of the wetting time of a solderable surface area as it ages Figure 6: Schematic diagram of the wetting time of a solderable surface area as it ages

During Stage I an oxide coating develops and solderability deteriorates: during Stage II, the wetting time stays constant, although the oxide continues to grow. The explanation proposed is that unsolderable oxide coatings are broken up by the flux action (rather than reduced to the metals) and then float away from the soldering site. The surface becomes unsolderable (stage III) once the oxide has become thick enough to prevent this happening.

Figure 7 relates the thickness of solderable coatings to their deterioration with time, which demonstrates the benefits of a thick coating.

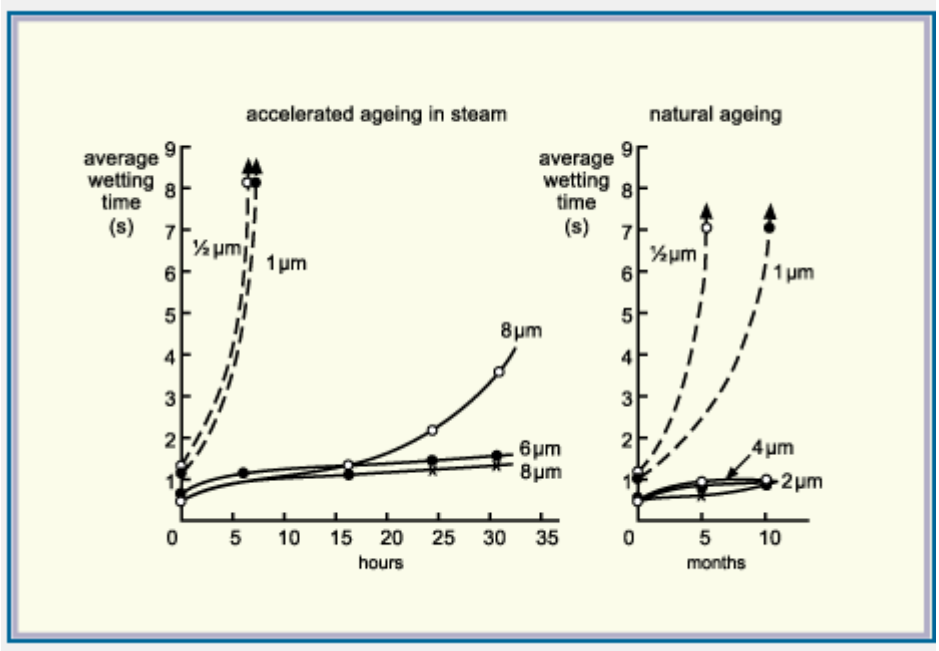


Figure 7: Wetting time vs ageing time for different coating thicknesses

As you would expect, given the fact that steam ageing accelerates effects that are found naturally in life, this technique has been used to demonstrate the ability of coatings to withstand atmospheric conditions. One would hope for good correlation between the performance of samples aged in steam and those that have been 'shelf-aged'. However, always take care when placing too much confidence in any technique:

Romm has criticised steam ageing as a means of evaluating the long-term performance of nickel-palladium finished lead frames, on the grounds that it inordinately affects the solderability test performance

Another ageing test performed in the electronics industry in order to simulate the long storage of process to boards is to carry out a 4-hour anneal at 155°C, intended to substitute for one year of storage at room temperature. Lamprecht criticises this test because it builds up a thicker layer of intermetallic compounds, and suggests that it is better to subject the parts to three reflow processes.

The wetting balance test deliberately uses a minimum amount of flux, in fact the mildest flux available. This is not necessarily representative of the performance of real products, where a more active flux may be available. As a designer, you need to know something of the materials used by your assembler, because there may be incompatibilities between certain combinations of fluxes and coatings. For example,

Electrochemicals report that not all no-clean fluxes may be compatible with OSP coatings.

SIR

Also known as insulation resistance (IR) or moisture and insulation resistance (M&IR) testing, Surface Insulation Resistance (SIR) testing is an industry-standard way of assessing the potential of a board to fail through corrosion and other processes associated with ionic contamination.

We shall come across this test regularly throughout this module, for the reason that increases in leakage current can effect the operation of most circuitry, particularly as operating currents are generally moving downwards.

As described in Fluxes for soldering, SIR is used to evaluate fluxes and cleaning processes, but SIR is also used for evaluating board finishes. The mechanisms relating to the surface finish that can cause failure during the test reflect both the material choice and the process conditions, in particular any ionic contamination remaining after the plating process.

To maximise the sensitivity of the test, leakage current is measured between long parallel lines at different electrical potentials. Instead of making very long and narrow circuits, electrically equivalent inter-digitated 'combs' are typically used, an example of which is shown in Figure 8.

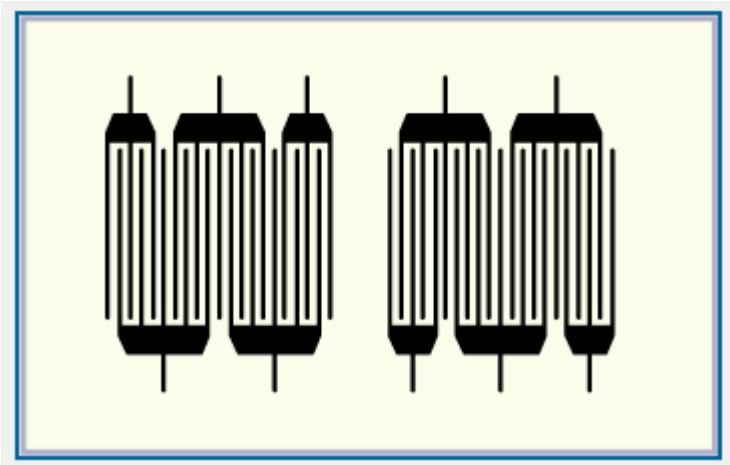


Figure 8: Sample SIR test pattern

The standards depend on application: telecommunications comb patterns have 0.63mm (0.025") lines and 1.27mm (0.050") gaps; the IPC1 'B' standard pattern has 0.31mm (0.0125") lines and spaces.

1 PDF files of the IPC standard Surface Insulation Resistance tests (IPC-TM-650 Method 2.6.3 series) may be downloaded free of charge at http://www.ipc.org/html/fsresources.htm

Traditionally, measurements are reported as insulation resistance (in ohms or Megohms) rather than as leakage current. This conversion is simple via Ohm's Law, V = I x R, where V is the test voltage and I is the leakage current. The diagrams in Figure 9 show typical circuitry used to apply a 45–50VDC bias voltage and to measure the resistance with a reverse polarity 100VDC test voltage.

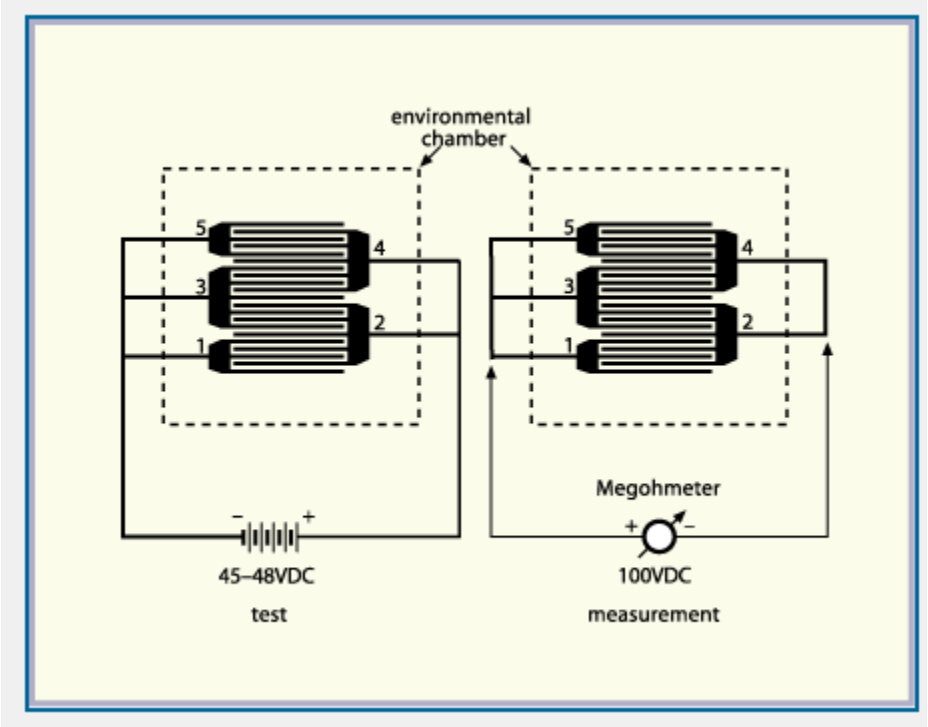


Figure 9: SIR test and measurement circuits

For most general cases, the SIR results will be a function of a number of parameters:

the inter-track spacing and length of the tracks

the test voltage and electrification time

the bias voltage

the ambient temperature and relative humidity

any temperature and/or humidity cycling which is carried out

the dielectric material of the test board and the properties of any solder resist coating.

Although all these parameters will greatly influence the results, changes in SIR can be used validly to compare different processes by using repeatable settings which are representative of the application. Some tests may simulate equipment life, while other tests are carried out with a 100VDC test voltage and a 45–50VDC bias of reverse polarity, in an ambient with 90–98%RH (relative humidity), and at temperatures of 55ºC, 65ºC or 85ºC, to accelerate the ageing of samples. However, it is important to realise that an extreme environment may cause some surfaces to fail by mechanisms that do not apply under normal operating conditions.

Typical SIR test regimes will look for a minimum of 100MW insulation resistance, both at the outset and after a period of exposure to a defined combination of voltage, temperature and humidity. As with all humidity tests, accurate measurements in situ are difficult to make, and parts may be removed from the chamber for testing. Also, for higher levels of humidity, where water absorbed or condensed on the surface may affect the insulation resistance measurement, it is not uncommon to specify a defined period of 'recovery' after exposure and before retesting. Common cumulative exposure periods are one, four and 21 days, with specimens that have acceptable insulation resistances being returned to the chamber after each retest, if they have been removed for testing.

Exposed copper

Exposed copper may be seen on an assembly when the molten solder has not fully wetted the pads or the corners of SMT footprints. This phenomenon may be caused by encroachment of the solder resist, or by ineffective surface coating.

The concern about exposed copper is that a corrosion cell might be set up, producing long-term unreliability. Under operating conditions of elevated temperature, humidity and bias, exposed copper could then corrode and reduce the insulation resistance of the assembly. However, electromigration studies of organic coatings exhibiting exposed copper showed no evidence of any electromigration, even after one thousand hours at applied voltages up to 500VDC at 85°C and 85%RH. Furthermore, DeBiase reported that the surface insulation resistance on the exposed copper panels was equivalent to that on the controls.

In the first part of this unit, we are concentrating on the main runners in the field of materials and finishes. Historically the two plated finishes described in the next two sections have accounted for the bulk of printed circuit boards manufactured, although process issues and environmental considerations are driving change in this area.

Later in this section, there will be much more information on a wider range of the available surface finishes. At this time, all you need to be aware of is that there are many options, and always reliability and cost issues, so you should talk to your board supplier before making a definite decision, and should seek sensible compromises.

Author: Martin Tarr

Source: http://www.ami.ac.uk/courses/topics/0130_sbf/index.html