POWER PLANNING

There are two types of power planning and management. They are **core cell power management** and **I/O cell power management**. In former one VDD and VSS power rings are formed around the core and macro. In addition to this straps and trunks are created for macros as per the power requirement. In the later one, power rings are formed for I/O cells and trunks are constructed between core power ring and power pads. Top to bottom approach is used for the power analysis of flatten design while bottom up approach is suitable for macros.

The power information can be obtained from the front end design. The synthesis tool reports static power information. Dynamic power can be calculated using **Value Change Dump (VCD)**or **Switching Activity Interchange Format (SAIF)** file in conjunction with RTL description and test bench. Exhaustive test coverage is required for efficient calculation of peak power. This methodology is depicted in Figure (1).

For the hierarchical design budgeting has to be carried out in front end. Power is calculated from each block of the design. Astro works on flattened netlist. Hence here top to bottom approach can be used. JupiterXT can work on hierarchical designs. Hence bottom up approach for power analysis can be used with JupiterXT. IR drops are not found in floor planning stage. In placement stage rails are get connected with power rings, straps, trunks. Now IR drops comes into picture and improper design of power can lead to large IR drops and core may not get sufficient power.

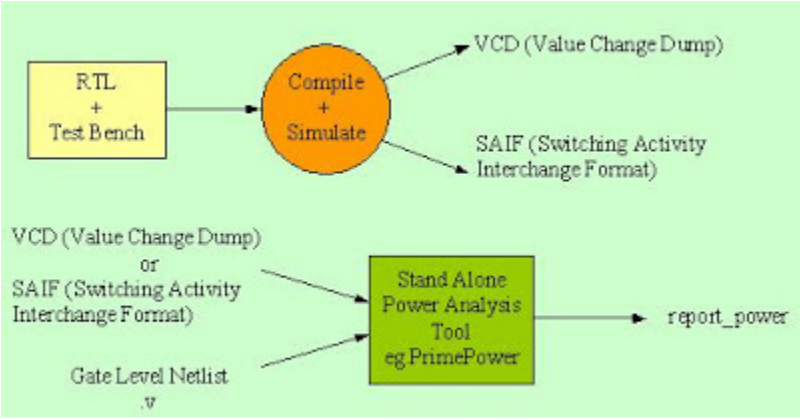

Figure (1) Power Planning methodology

Below are the calculations for flattened design of the SAMM. Only static power reported by the Synthesis tool (Design Compiler) is used instead of dynamic power.

- **The number of the core power pad required for each side of the chip**

= total core power / [number of side*core voltage*maximum allowable current for a I/O pad]

= 236.2068mW/ [4 * 1.08 V * 24mA] (Considering design SAMM)

= 2.278

~ 2

Therefore for each side of the chip 2 power pads (2 VDD and 2 VSS) are added.

- **Total dynamic core current (mA)**

= total dynamic core power / core voltage

= 236.2068mW / 1.08V

= 218.71 mA

- **Core PG ring width**

= (Total dynamic core current)/ (No. of sides * maximum current density of the metal layer used (Jmax) for PG ring)
=218.71 mA/(4*49.5 mA/µm)
~1.1 µm
~2 µm

- **Pad to core trunk width (µm)**

= total dynamic core current / number of sides * J_{max} where Jmax is the maximum current density of metal layer used

= 218.71 mA / [4 * 49.5 mA/µm]

= 1.104596 µm

Hence pad to trunk width is kept as 2µm.

Using below mentioned equations we can calculate vertical and horizontal strap width and required number of straps for each macro.

- Block current:

$$I_{block} = P_{block} / V_{ddcore}$$

- Current supply from each side of the block:

$$I_{top} = I_{bottom} = \{ I_{block} * [W_{block} / (W_{block} + H_{block})] \} / 2$$

$$I_{left} = I_{right} = \{ I_{block} * [H_{block} / (W_{block} + H_{block})] \} / 2$$

- Power strap width based on EM:

$$W_{strap\_vertical} = I_{top} / J_{metal}$$

$$W_{strap\_horizontal} = I_{left} / J_{metal}$$

- Power strap width based on IR:

$$W_{strap\_vertical} >= [I_{top} * R_{oe} * H_{block}] / 0.1 * VDD$$

$$W_{strap\_horizontal} >= [I_{left} * R_{oe} * W_{block}] / 0.1 * VDD$$

- Refresh width:

$$W_{refresh\_vertical} = 3 * \text{routing pitch} + \text{minimum width of metal (M4)}$$

$$W_{refresh\_horizontal} = 3 * \text{routing pitch} + \text{minimum width of metal (M3)}$$

- Refresh number

$$N_{refresh\_vertical} = \max (W_{strap\_vertical}) / W_{refresh\_vertical}$$

$N_{refresh\_horizontal} = max (W_{strap\_horizontal}) / W_{refresh\_horizontal}$

- Refresh spacing

$S_{refresh\_vertical} = Wblock / N_{refresh\_vertical}$

$S_{refresh\_horizontal} = Hblock / N_{refresh\_horizontal}$

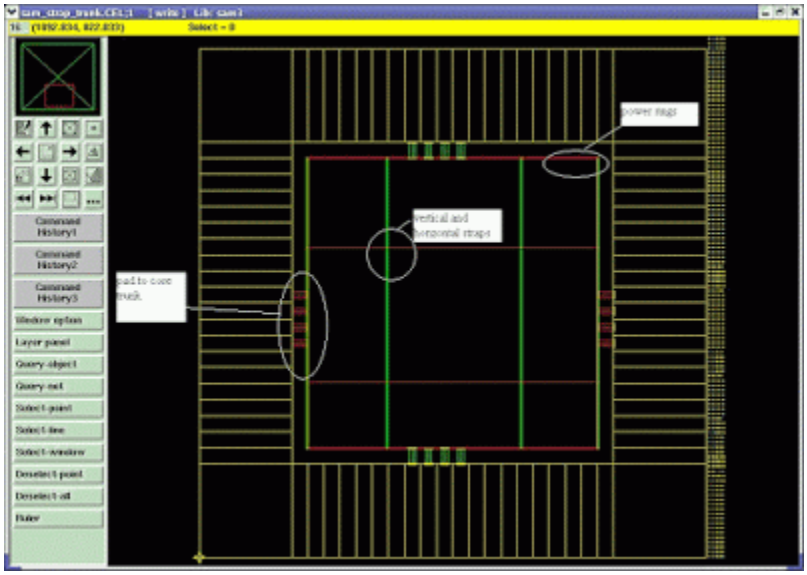

Figure (2) Showing core power ring, Straps and Trunks

Source : http://asic-soc.blogspot.in/2007/10/power-planning.html