Optimization of Gate – Source/Drain Underlap on 30 nm Gate Length FinFET Based LNA Using TCAD Simulations

K.K.NAGARAJAN[1], N.VINODHKUMAR[2] and R.SRINIVASAN[2]
[1]Department of Computer Applications
[2]Department of Information Technology
SSN College of Engineering
Rajiv Gandhi Salai, Kalavakkam - 603110
INDIA
nagarajankk@ssn.edu.in, vinodhkumar.cc@gmail.com, srinivasanr@ssn.edu.in
http://www.somca.ssn.edu.in/department-mca-faculty-nagarajan.php

Abstract: - The effect of gate – drain/source underlap (L_{un}) on a narrow band LNA performance has been studied, in 30 nm FinFET using device and mixed mode simulations. Studies are sssssdone by maintaining and not maintaining the leakage current (I_{off}) and threshold voltage (V_{th}) of the various devices. LNA circuit with two transistors in a cascode arrangement is constructed and the input impedance, gain and noise-figure have been used as performance metrics. To get the better noise performance and gain, L_{un} in the range of 3-5nm is recommended.

Key-Words: - FinFET, LNA, TCAD, Underlap, Noise-Figure, Gain

1 Introduction

Drain induced barrier lowering (DIBL) and Short channel effects (SCE) are becoming the fundamental limiting factors in scaling of a single gate planar CMOS transistor. FinFETs are emerging as a potential alternative to MOSFETs due to their quasi planar structure and compatibility with CMOS technology. FinFET, a recently reported novel double-gate structure, the Si fin forms the channel and gate wraps around the fin. The Si fin has insulator on top and gate on either side, current flows parallel to the device surface. In ref. [1] FinFETs fabricated with a channel length of 45 nm have been used to build low and high frequency analog applications, including low noise amplifier (LNA).

LNA is a key component in RF front-end receivers which poses a major challenge in terms of meeting high gain and low noise figure at low power supply voltages. Abundant literature is available for MOSFET-based LNA. FinFET-based LNA is of current research interest and is being investigated in many studies [1] – [7]. FinFETs of channel lengths of 90 nm [2] and 45 nm [1] are used to construct LNA. Various studies of DG FinFETs [8]-[10] intimated performance benefits of gate-source/drain underlap, and suggested it could underlie optimal nanoscale design. In this paper, a FinFET based LNA has been designed and the effect of underlap (L_{un}) on LNA parameters such as input impedance (Z_{IN}), gain (S_{21}) and noise figure (NF) have been studied using TCAD simulator. This paper presents a LNA design using 30 nm FinFET and the effect of underlap on LNA performance. In the next section, TCAD simulator and the simulation methodology have been discussed. Simulation results are discussed in the section 3. Finally, section 4 gives the conclusion.

2 Simulator and Simulation Methodologies

2.1 Simulator

Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE) and Sentaurus Mesh (SNMESH): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations
- Inspect and Tecplot: To view the results.

Mixed mode simulation facility of SDEVICE is used to investigate the performance of LNA. The

mode simulation of LNA circuit (Fig. 4). Transistors M1 and M2 are simulated at the device level. Other elements are simulated using the compact models at the circuit level. M1 and M2 are identical transistors. Inductors, L_g and L_o, are used with their series resistance incorporated, and a quality factor of 5 is assumed. Resistances associated with the inductors are given by the following familiar expression

$$R = \frac{2\pi f \times inductor\ value}{quality\ factor} \quad (1)$$

The circuit is operated at the supply voltage of V_{dd} = 1 V, V_{gs} of M1 = 0.5 V and L_o = 1.5 nH. The operating frequency (f) of LNA is taken as 10 GHz.

The standard AC simulations are done over a range of frequencies. SDEVICE outputs are in the form of admittance and capacitance matrices. They are converted to **S** parameter and $\mathbf{S_{21}}$ is taken as gain of LNA.

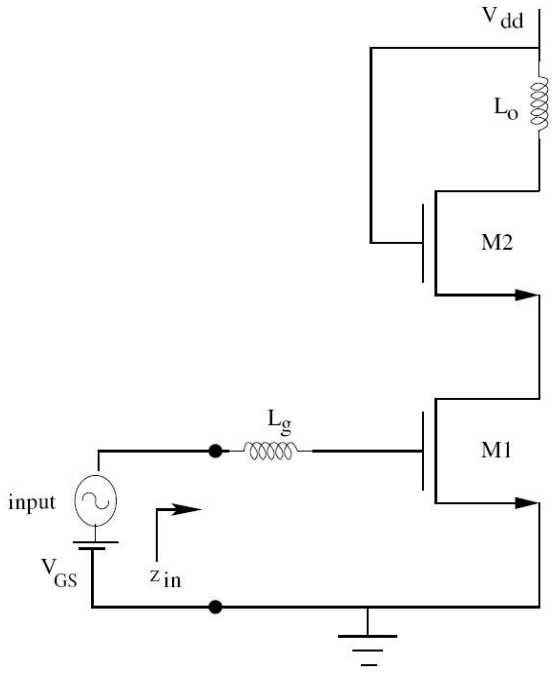

Fig. 4 LNA circuit used in this study

Noise simulation in SDEVICE is standard AC simulation with noise models included in the physics section. Noise-figure (NF) calculation is done by assuming a signal source resistance (purely resistive) of 50Ω.

For a two port network NF is defined as [13]-[15],

$$NF = 1 + \frac{1}{S_I^S}\left(S_I^{gg} + |\alpha|^2 S_I^{dd} - 2\mathrm{Re}\left(\alpha S_I^{dg}\right)\right) \quad (2)$$

with $$\alpha = \frac{Y_S + Y_{11}}{Y_{21}} \quad (3)$$

where S_I^S is the current noise spectrum of the noisy source admittance and is given by

$$S_I^S = 4k_B T\mathrm{Re}\,(Y_S) \quad (4)$$

S_I^{gg} and S_I^{dd} are the current noise spectrums, at the gate and drain terminals respectively, S_I^{dg} is the cross-correlation noise spectra between the drain and gate terminals, Y_{11} and Y_{21} are the respective admittance (Y) parameters.

When the underlap is changed, the effect is reflected in the device level (I_{off}, I_{on}, V_{th}, f_t, g_m etc.) as well as in the circuit level (LNA performance metrics such as input impedance, gain, and noise figure). (Refer Fig. 5a and Fig. 6). This gives rise to two philosophies i.e. studying LNA parameters with and without matching the device level parameters. Matching either I_{off} or V_{th} can be seen as a fair comparison (Refer Fig. 5b). Keeping the above points in mind, following three case studies are constructed and LNA performance is studied.

- Case 1: Underlap is changed without matching neither I_{off} nor V_{th}
- Case 2: Underlap is changed with I_{off} matching
  - I_{off} matching through gate electrode work function(WF)
  - I_{off} matching through channel doping (N_{ch})
- Case 3: Underlap is changed with V_{th} matching
  - V_{th} matching through gate electrode work function(WF)
  - V_{th} matching through channel doping (N_{ch})

3 Results and Discussion

As stated earlier, change in L_{un} causes variations in device parameters. When L_{un} is changed, the device parameters like I_{on}, I_{off}, V_{th} etc., gets affected. Therefore the device is characterized initially, which is followed by the LNA characterization. Fig. 5a shows the plots of I_{on} versus underlap and I_{off} versus underlap. As L_{un} is increased, the series resistance associated with the channel increases thereby

reducing the leakage current (I_{off}) which can be observed in Fig. 5a.

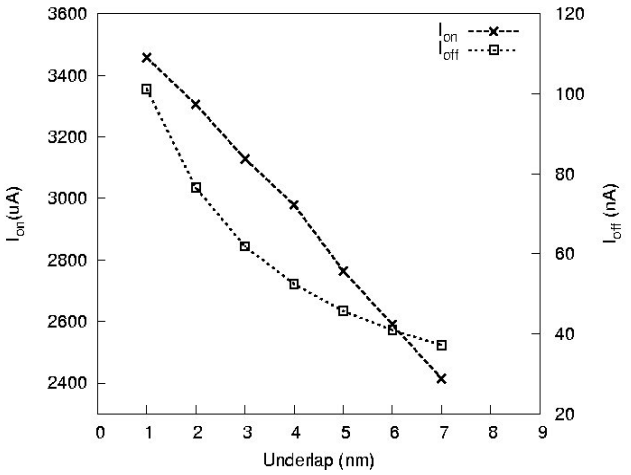

Fig. 5a Effect of L_{un} on I_{off} and I_{on}

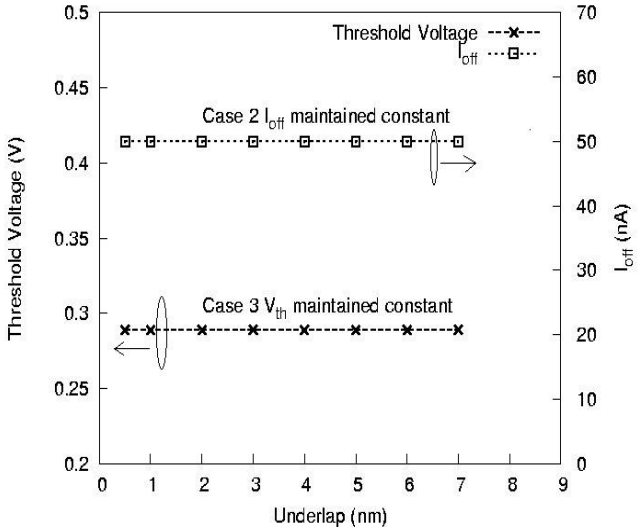

Fig. 5b V_{th} or I_{off} maintained constant (through N_{ch} or WF) with respect to underlap for fair comparison

When L_{un} of the FinFET device used in LNA circuit varies, it not only affects the device level parameters, it also affects circuit level parameters like real and imaginary part of the input impedance, gain and NF.

Next the effect of L_{un} at the circuit level is considered. To do this, using 0.5 nm as L_{un} and other parameter as shown in Table I, a FinFET is generated. Using this device, LNA simulation is done in SDEVICE simulator and the mixed mode simulation approach is followed. Appropriate values of gate inductor and transistor width provide an input impedance of 50 Ω (purely real). After input impedance matching, the gain and NF are extracted. The simulation results, gain (S_{21}) = 9.21 dB, and noise-figure (NF) =1.977 dB are matching with the experimental results [1 and 15]. FinFETs with different L_{un}s are created which is followed by LNA simulations. Fig. 6 shows the input impedance, both real and imaginary, as a function of L_{un}. It can be seen from Fig. 6 that both real and imaginary part of the input impedance increases when L_{un} increases. The input impedance of LNA circuit shown in Fig. 4 is given by,

$$Z_{in} = R_{Lg} + R_g + r_i \qquad (5)$$

where R_{Lg} is the resistance due to gate inductor, R_g is the intrinsic gate resistance, and r_i is due to NQS effect. If we assume proper layout technique have been adopted R_g can be ignored. Since r_i increases with L_{un} [16], the real part of the input impedance increases with L_{un}.

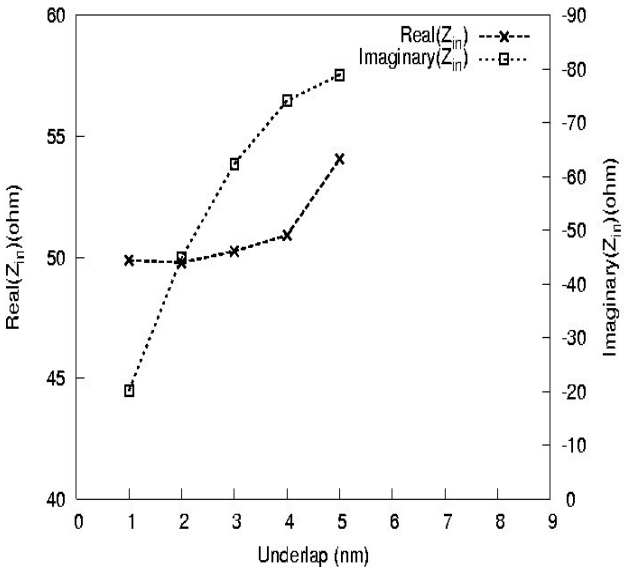

Fig. 6 Real and Imaginary part of input impedance versus underlap of the device

C_{geff} in DGMOS can be expressed as [17],

$$C_{geff} = \text{Series}\,(C_{ox}, C_{si}) \,||\, C_{ov} \,||\, C_{fringing} \qquad (6)$$

where C_{ox} is the oxide capacitance, C_{si} is the silicon body capacitance, C_{ov} is the gate to source/drain overlap capacitance and $C_{fringing}$ is the fringing capacitance. In our device C_{ov}=0 because no overlap exists between gate and source/drain. $C_{fringing}$ is given by [18],

$$C_{fringing} = \frac{k\varepsilon_{di}W}{\pi} \ln \frac{\pi W}{\sqrt{L_{un}^2 + T_{ox}^2}} e^{-\left|\frac{L_{un}^2 - T_{ox}^2}{L_{un}^2 + T_{ox}^2}\right|} \qquad (7)$$

For the given transistor width (W), as per (7) when L_{un} increases, $C_{fringing}$ decreases, which in turn decreases the C_{geff} with the increased capacitive reactance. So the imaginary part of the input impedance increases with L_{un}.

3.1 Case 1

It has been seen that the change in L_{un} affects the device level parameters such as I_{on}, I_{off}, V_{th} as well as circuit level parameters such as input impedance, gain and NF. Case 1 focuses on the procedure where the underlap is changed without matching neither I_{off} nor $V_{th.}$ When L_{un} is changed the input impedance can be matched by adjusting the gate inductor and the width of the transistor. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real, are shown in Table 2. Since real part of the input impedance increases with L_{un} (Fig. 6), we need larger transistor widths to achieve 50 Ω, real part. Again it may be recollected from Fig. 6 that L_{un} increases the input capacitive reactance (i.e. imaginary part of input impedance) thereby demanding higher gate inductor values. But it can be noticed from Table 2 that after 4 nm of L_{un} the required gate inductor value decreases. For higher L_{un} s, larger transistor widths are needed to make real part of the input impedance equal to 50 Ω. But this procedure at some point makes C_{geff} to go up i.e. we need smaller gate inductors to cancel out the capacitive reactance. In our simulation, this happens when L_{un} = 4 nm (refer Table 2).

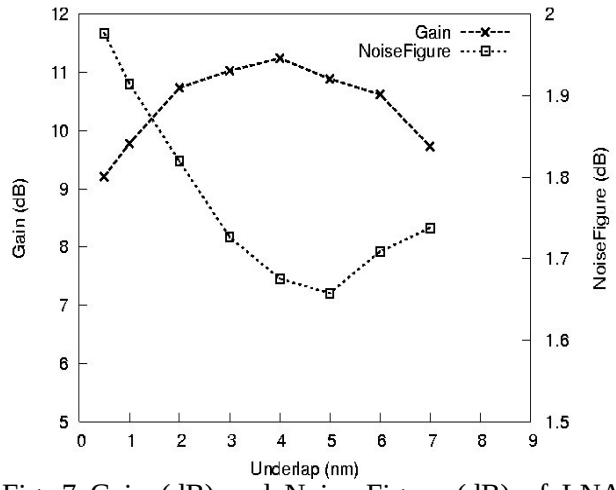

Fig. 7 Gain (dB) and Noise Figure (dB) of LNA after getting a 50 Ω input impedance match at 10 GHz, for different underlaps

Table 2 Values of L_{un}, L_g, f_t, Width and their respective Gain, Noise figure (I_{off} not maintained)

L_{un} in nm	Gate inductor (L_g) (nH)	f_t (GHz)	Width of the transistor (μm)	Gain (S_{21}) (dB)	NF (dB)
0.5	1.35	735.7	16	9.21	1.97
1	1.55	815.1	17	9.77	1.91
2	1.75	881.4	19	10.73	1.82
3	1.90	889.7	20	11.02	1.72
4	1.95	888.4	21	11.24	1.67
5	1.90	854.4	22	10.88	1.66
6	1.70	829.3	24	10.62	1.71
7	1.55	801.7	25	9.73	1.74

From Fig. 7 it is observed that the gain of the LNA is going through a peak i.e. the gain increases and then decreases with respect to L_{un}. A maximum gain value of 11.243 dB occurs at L_{un}= 4nm. On one hand, the increased transistor width used with increased L_{un}, enhances g_m and thereby the gain. But on another hand increased L_{un} increases the series resistance and thereby degrades g_m at some point which in turn lowers the gain. In essence, for lower values of L_{un}, increase in the transistor width is responsible for increase in g_m and the decrease in $C_{fringing}$ is responsible for the decrease in C_{geff} and at higher values of L_{un}, increase in the series resistance is responsible for g_m degradation and the increase in the transistor width increases $C_{fringing}$ which is responsible for the increase in C_{geff}.

From Fig. 7 it can be noticed that NF travels through a minima when L_{un} is varied. Around L_{un}=4 nm a minimum value of NF is achieved. Let us consider the input stage of Fig.4. We have a common source amplifier, with an inductor and resistor (includes the parasitic resistance of the inductor) at the gate. Noise-Figure of this stage alone is given by [19],

$$NF = 1 + \left(\frac{f_o}{f_t}\right)K \quad (8)$$

where f_o – resonant frequency, f_t – unity gain frequency, and K – noise factor scaling coefficient, and depends on the resonant frequency, quality factor of the inductor, $\frac{g_{d0}}{g_m}$ ratio (g_m – transconductance of the FinFET, g_{d0} – output conductance of the FinFET at zero drain bias) and process specifications.

Equation (8) tells that NF is decided by K and f_t once we fix the frequency of operation or resonant frequency. As already discussed g_m increases whereas C_{geff} decreases for L_{un} values up to 4nm, after which they reverse the trend. It is well known that f_t is directly proportional to g_m and inversely proportional to C_{geff}. Therefore, f_t increases up to L_{un}=4 nm and then starts decreasing (refer Table 2). This causes NF to decrease and then increase when L_{un} is increased.

3.2 Case 2

When L_{un} is varied it not only affects the input impedance of LNA but also affects the device leakage (I_{off}). When L_{un} is increased both I_{off} and I_{on} decrease. To have a fair comparison between the devices with different L_{un}s, a constant I_{off} constraint can be superimposed. When L_{un} of the device is varied, I_{off} is maintained around 50 nA. To achieve this either channel doping (N_{ch}) or gate electrode work function (WF) can be adjusted. When N_{ch} is used as a means of achieving I_{off} constraint, gate electrode work function is maintained at 4.336eV. Similarly when gate electrode work function is used as a means of achieving I_{off} constraint, N_{ch} is fixed at a value of 1.1e18 per cm^3.

Once again, when L_{un} is changed the input impedance matching was achieved by adjusting the gate inductor and transistor width. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real are shown in Table 3. It also gives WF, f_t of the various devices, and their respective gain and noise figure values.

Fig. 8 depicts the gain and NF against L_{un} when I_{off} constraint is maintained through gate electrode work function and it can be noticed from Fig. 8 that both the gain and NF have some optimum L_{un} i.e. around L_{un} = 4 nm, we get 12.1 dB gain and 0.96 dB NF. On one hand, the increased transistor width used with increased L_{un}, enhances g_m and thereby the gain. But on another hand increased L_{un} increases the series resistance and thereby degrades g_m at some point which in turn lowers the gain.

In essence, for lower values of L_{un}, increase in the transistor width is responsible for increase in g_m and the decrease in $C_{fringing}$ is responsible for the decrease in C_{geff} and at higher values of L_{un}, increase in the series resistance is responsible for g_m degradation and the increase in the transistor width increases $C_{fringing}$ which is responsible for the increase in C_{geff}.

Equation (8) tells that NF is decided by K and f_t once we fix the frequency of operation or resonant frequency. As already discussed g_m increases whereas C_{geff} decreases for L_{un} values up to 4nm, after which they reverse the trend. It is well known that f_t is directly proportional to g_m and inversely proportional to C_{geff}. Therefore, f_t increases up to L_{un}=4 nm and then starts decreasing (refer Table 3). The behaviour of the gain and NF shown in Fig. 8 is same as Fig. 7 of case 1.

Table 3 Values of L_{un}, WF, f_t, Gate Inductor (L_g), Width of the transistor (W) and their respective Gain, Noise figure (I_{off} maintained through gate electrode WF)

L_{un} in nm	WF in eV	f_t in GHz	L_g in nH	W in µm	Gain (S_{21}) (dB)	NF (dB)
0.5	4.336	737	1.45	16	9.39	1.10
1	4.334	815	1.65	17	9.97	1.04
2	4.324	866	1.9	19	11.0	0.98
3	4.317	866	2.05	20	11.4	0.98
4	4.312	841	2.05	22	12.1	0.96
5	4.307	812	2.05	23	11.8	0.99
6	4.304	774	1.95	24	11.2	1.03
7	4.301	737	1.75	26	10.6	1.07

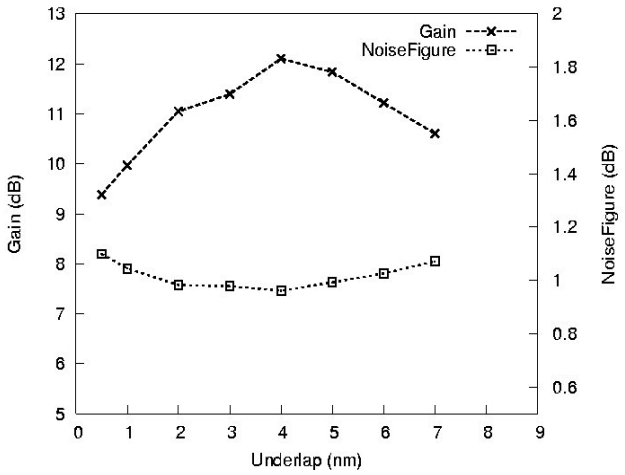

Fig. 8 Gain(dB) and Noise Figure(dB) of LNA after getting a 50Ω input impedance match at 10 GHz, for different underlaps with I_{off} = 50 nA (maintained through gate work function)

The I_{off} constraint of the FinFET devices can also be achieved through channel doping (N_{ch}) as a function of varying L_{un}. Once again, when L_{un} is changed the input impedance matching was achieved by adjusting the gate inductor and transistor width. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real are shown in Table 4. It also gives N_{ch}, f_t of the various devices, and their respective gain and noise figure values.

Table 4 Values of L_{un}, N_{ch}, f_t, Gate Inductor (L_g), Width and their respective Gain, Noise figure (I_{off} maintained through channel doping)

L_{un} in nm	N_{ch} (per cm^3)	f_t GHz	(L_g) (nH)	W in µm	Gain (S_{21}) (dB)	NF (dB)
0.5	1.1e18	737	1.45	16	9.39	1.10
1	1e18	816	1.65	17	9.98	1.05
2	0.6e18	878	1.8	19	10.9	1.05
3	0.3e18	893	1.95	20	11.2	1.16
4	0.2e17	890	1.95	21	11.3	1.62
5	1e14	845	1.85	23	10.2	1.79

Fig. 9 depicts the gain and NF against L_{un} when I_{off} constraint is maintained through channel doping and it can be noticed from Fig. 9 that a maximum value of gain can be achieved at around L_{un}= 4 nm. Around L_{un}= 3 nm a minimum value of NF is achieved. We get a maximum gain of 11.3 dB and a minimum noise figure of 1.05 dB. The behaviour of the gain and NF shown in Fig. 9 is same as Fig. 7 of case 1. It can be reasoned out in the same manner as in case 1.

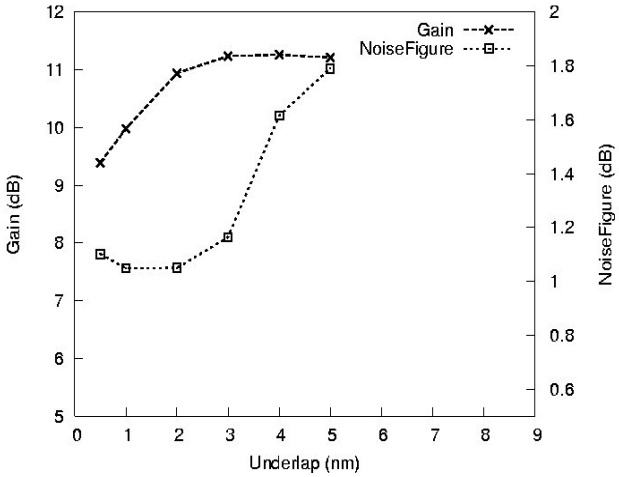

Fig. 9 Gain(dB) and Noise Figure(dB) of LNA after getting a 50Ω input impedance match at 10 GHz, for different underlaps with I_{off} = 50 nA (maintained through channel doping)

3.3 Case 3

It has been seen that when L_{un} is varied it not only affects the input impedance of LNA but also affects the threshold voltage (V_{th}). The study can also be made by matching V_{th} instead of I_{off}. When L_{un} of the device is varied, V_{th} is maintained around 0.288 volts and once again the gate electrode work function (WF) or channel doping (N_{ch}) can be adjusted to achieve this constraint.When L_{un} is changed the input impedance matching was achieved by adjusting the gate inductor and transistor width. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real are shown in Table 5. It also gives WF of the various devices, and their respective gain and noise figure values.

From Fig. 10 it is observed that the gain of the LNA is going through a peak i.e. the gain increases and then decreases with respect to L_{un}. A maximum gain value of 11.79 dB occurs at L_{un}= 5 nm, which can be reasoned out in the same manner as in case 1.

Table 5 Values of L_{un}, WF, Gate Inductor (L_g), Width and their respective Gain, Noise figure (V_{th} maintained throughWF)

L_{un} in nm	WF in eV	L_g in nH	W in µm	Gain (S_{21}) (dB)	NF (dB)
1	4.336	1.65	17	9.96	1.04
2	4.332	1.85	19	10.96	0.959
3	4.329	2.0	20	11.29	0.936
4	4.312	2.075	21	11.58	0.922
5	4.326	2.0	23	11.79	0.895
6	4.326	1.925	24	11.33	0.913
7	4.329	1.75	25	10.45	0.935

From Fig. 10 it can be noticed that NF travels through a minima when L_{un} is varied. Around L_{un}=5 nm a minimum value of NF is achieved. The behaviour of the gain and NF shown in Fig. 10 is similar to Fig. 7 of case 1. It can be reasoned out in the same manner as in case 1.

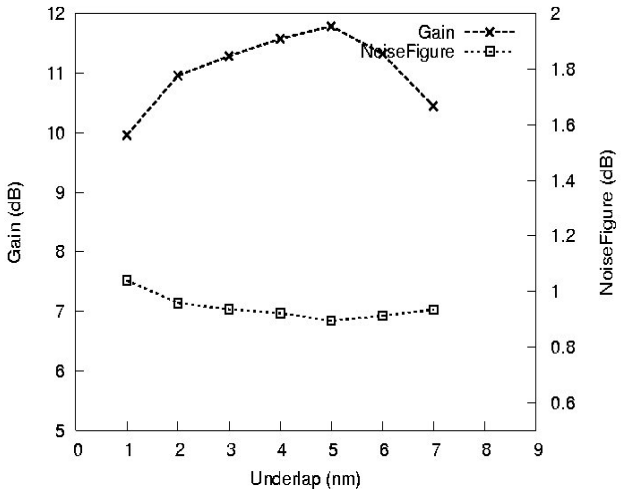

Fig. 10 Gain (dB) and Noise Figure (dB) of LNA after getting a 50 Ω input impedance match at 10 GHz, for different underlaps with V_{th} = 0.288 V (maintained through gate work function)

The V_{th} constaint of the FinFET devices can also be achieved through channel doping (N_{ch}) as a function of varying $L_{un.}$ Once again, when L_{un} is changed the input impedance matching was achieved by adjusting the gate inductor and transistor width. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real are shown in Table 6. It also gives N_{ch} of the various devices, and their respective gain and noise figure values.

Table 6 Values of L_{un}, N_{ch}, Gate Inductor (L_g), Width and their respective Gain, Noise figure (V_{th} maintained through N_{ch})

L_{un} in nm	N_{ch} (per cm^3)	L_g (nH)	W in µm	Gain (S_{21}) (dB)	NF (dB)
1	11e17	1.65	17	9.96	1.04
2	10e17	1.85	19	10.95	0.957
3	9.2e17	2.0	20	11.27	0.934
4	8.7e17	2.05	21	11.54	0.919
5	8 e17	2.05	22	11.38	0.928
6	8.7e17	1.9	24	11.36	0.906
7	9.2e17	1.7	25	10.52	0.927

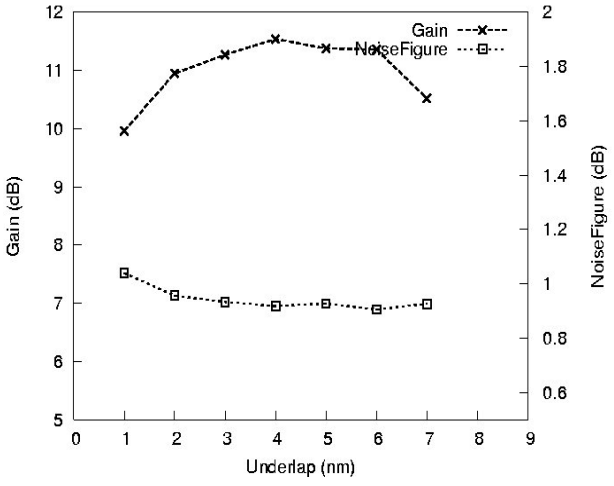

Fig. 11 Gain (dB) and Noise Figure (dB) of LNA after getting a 50 Ω input impedance match at 10 GHz, for different underlaps with V_{th} = 0.288 V (maintained through channel doping)

Fig. 11 depicts the gain and NF against L_{un}, when V_{th} constraint is maintained through channel doping for different underlap devices and it can be noticed from Fig. 11 that both the gain and NF have some optimum L_{un} i.e. around L_{un} = 4 nm, we get 11.54 dB gain and 0.919 dB NF. The behaviour of the gain and NF shown in Fig. 11 is same as Fig. 7 of case 1. It can be reasoned out in the same manner as in case 1.

4 Conclusion

In this paper, we have investigated the effect of L_{un} on gain and NF of a 10 GHz, narrow band LNA using TCAD simulations. Changing L_{un} was followed by two philosophies, not maintaining I_{off} and maintaining I_{off}. When I_{off} was not maintained, a maximum gain of 11.243 dB was achieved at L_{un}= 4 nm and a minimum NF of 1.657 dB was achieved at L_{un}=5 nm. When I_{off} was maintained around 50 nA through work function, a maximum gain of 12.105 dB and a minimum NF of 0.962 dB at L_{un}= 4 nm. When I_{off} was maintained around 50 nA through channel doping, a maximum gain of 12.105 dB and a minimum NF of 0.962 dB at L_{un}= 4 nm. L_{un} around 4 nm gives an optimum performance between the gain and NF, 11.54 dB and 0.919dB respectively, when V_{th} is maintained through N_{ch}. L_{un} around 5 nm gives an optimum performance between the gain and NF, 11.79 dB and 0.895dB respectively, when V_{th} is maintained through WF. L_{un} in the range of 3-5nm will give optimum gain and NF for this LNA design.

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References:

[1] Piet Wambacq, Bob Verbruggen, Karen Scheir, Jonathm Borremans, Mortin Dehan, Dimitri Linten, Vincent De Heyn, Geert Van der Plas, Abdelkarim Mercha, Bertrand Parvais, Cedric Gustin, Vaidy Subramanian, Nadine Collaert, Malgorzata Jurczak and Stefaan Decoutere, The Potential of FinFETs for Analog and RF Circuit Applications, *IEEE Transactions on Circuits and Systems-I*, 54 (11), Nov 2007.

[2] D Linten, X Sun, S Thijs, M I Natarajan, A Mercha, G Carchon, P Wampbacq, T Nakaie and S Decoutere, Low-power Low-noise Highly ESD Robust LNA, and VCO Design Using Above-IC Inductors, *IEEE 2005 Custom Intergated Circuits Conference* 14-3-1, 2005.

[3] J. Borremans, B. Parvais, M. Dehan, S. Thijs, P. Wambacq, A. Mercha, M. Kuijk, G. Carchon and S. Decoutere, Perspective of RF design in future planar and FinFET CMOS, *IEEE Radio Frequency Integrated Circuits Symposium*, 2008

[4] Sebastien Nuttinck, Bertrand Parvais, Gilberto Curatola, and Abdelkarim Mercha, Double-Gate finFETs as a CMOS Technology Downscaling Option: An RF Perspective, *IEEE Transactions on Electron Devices*, Vol. 54, No. 2, February 2007.

[5] G. Knoblinger, F. Kuttner, A. Marshall, C. Russ, P. Haibach, P. Patruno, T. Schulz, W. Xiong, M. Gostkowski, K. Schruefer, and C.R. Cleavelin, "Design and evaluation of basic analog circuits in an emerging MuGFET technology," in *Proc. IEEE International SOI Conference*, Oct. 2005, pp. 39–40

[6] V. Kilchytska, N. Collaert, R. Rooyackers, D. Lederer, J.-P. Raskin and D. Flandre, Perspective of FinFETs for analog applications, in *Proceedings of 34th European Solid-State Device Research Conerence*, Sep. 2004, pp. 65–68.

[7] G. Knoblinger, M. Fulde, D. Siprak, U. Hodel, K. Von Arnim, Th. Schulz, C. Pacha, U. Baumann, A. Marshall, W. Xiong, C. R. Cleavelin, P. Patruno and K. Schruefer, Evaluation of FinFET RF Building Blocks, *Proceedings of IEEE International SOI Conference*, 2007

[8] Vishal Trivedi, Jerry G. Fossum, and Murshed M. Chowdhury, Nanoscale FinFETs with Gate-Source/ Drain Underlap, *IEEE Transcations on Electron Devices*, Vol. 52, No. 1, January 2005

[9] J.G. Fossum *et al.*, Physical insights on design and modeling of nanoscale FinFETs, in *IEDM Technical Digest*, 2003, pp. 679–682.

[10] Ji-Woon Yang, Peter M. Zeitzoff and Hsing-Huang Tseng, Highly manufacturable Double-Gate FinFET with Gate-Source/Drain Underlap, *IEEE Transcations on Electron Devices*, Vol. 54, No. 6, June 2007.

[11] Bin Yu, Leland Chang, Shibly Ahmed, Haihong Wang, Scott Bell, Chih-Yuh Yang, Cyrus Tabery, Chau Ho, Qi Xiang, Tsu-Jae King, Jeffrey Bokor, Chenming Hu, Ming-Ren Lin, and David Kyse, FinFET Scaling to 10 nm Gate Length, *IEDM*, 2002.

[12] Hau-Yiu Tsui and Jack Lau, SPICE simulation and tradeoffs of CMOS LNA performance with source-degeneration inductor, *IEEE Transactions On Circuits and Systems-II: Analog and Digital Signal Processing*, 47(1): 62-65, Jan 2000.

[13] Bernhard SCHMITHUSEN, Andreas SCHENK, and Wolfgang FICHTNER, Simulation of noise in semiconductor devices with dessis-ISE using the direct impedance field method, *Technical report*, 2000/08, June 2000.

[14] Andreas SCHENK, Bernhard SCHMITHUSEN, Andreas WETTSTEIN, Axel ERLEBACH, Simon BRUGGER, Fabian.M.BUFLER, Thomas FEUDEL, and wolfgang FICHTNER, Simulation of RF noise in MOSFETs using different transport models, *IEICE Transactions on Electronics*, E86-C(3):481-489, March 2003.

[15] Jean-Pierre Raskin, Guillaume Ailloncy, Dimitri Lederer, Francois Danneville, Gilles Dambrine, Stefaan Decoutere, Abdelkarim Mercham and Bertrand Parvais, High Frequency Noise Performance of 60-nm Gate-Length FinFETs, *IEEE Transactions on Electron Devices* 55 (10), Oct 2008.

[16] Yuhua Cheng and Mishel Matloubian, High frequency characterization of gate resistance in RF MOSFETs, *IEEE Electron Device Letters*, 22(2): 28-30, Feb 2001.

[17] Fathipour Morteza, Nematian Hamed, Kohani Fatemeh, The impact of structural parameters on the electrical characteristics of nano scale DG-SOI MOSFETs in subthreshold region, *4th International Conference: Sciences of Electronic, Technologies of Information and Telecommunications (SETIT 2007)*, Tunisia, March 25-29, 2007.

[18] R.Shrivastava and K.Fitzpartick, A simple model for the overlap capacitance of a VLSI MOS device, *IEEE Transactions on Electron Devices*, Vol.ED-29, pp.1870-1875, 1982.

[19] Elkim Roa, Joao Navarro Soares and Wilhelmus Van Noije, A Methodology for CMOS Low Noise Amplifier Design, *16th Symposium on Integrated Circuits and System Design*, SBCCI 2003