Module 1

Power Semiconductor Devices

Lesson 6

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Constructional Features, operating principle and characteristics of Power Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

Instructional Objectives

On completion the student will be able to

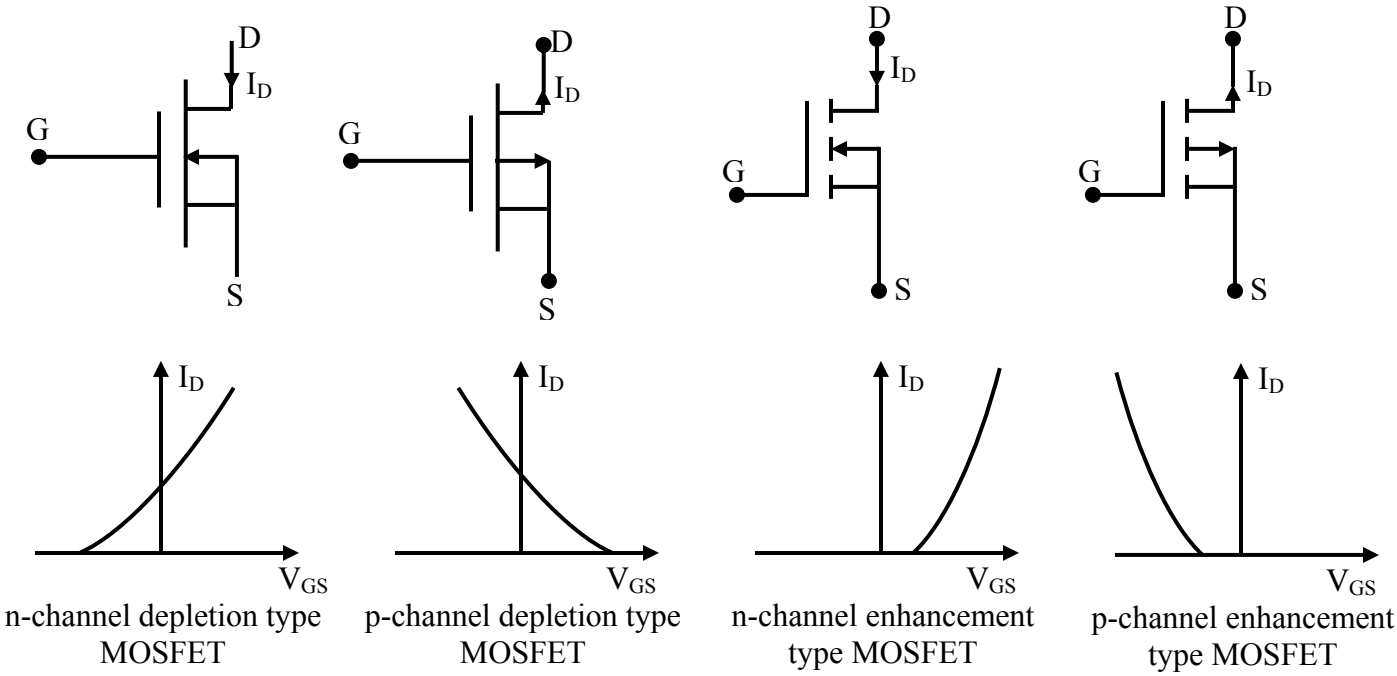
- Differentiate between the conduction mechanism of a MOSFET and a BJT.
- Explain the salient constructional features of a MOSFET.
- Draw the output i-v characteristics of a MOSFET and explain it in terms of the operating principle of the device.
- Explain the difference between the safe operating area of a MOSFET and a BJT.
- Draw the switching characteristics of a MOSFET and explain it.
- Design the gate drive circuit of a MOSFET.
- Interpret the manufacturer's data sheet rating of a MOSFET.

6.1 Introduction

Historically, bipolar semiconductor devices (i.e, diode, transistor, thyristor, thyristor, GTO etc) have been the front runners in the quest for an ideal power electronic switch. Ever since the invention of the transistor, the development of solid-state switches with increased power handling capability has been of interest for expending the application of these devices. The BJT and the GTO thyristor have been developed over the past 30 years to serve the need of the power electronic industry. Their primary advantage over the thyristors have been the superior switching speed and the ability to interrupt the current without reversal of the device voltage. All bipolar devices, however, suffer from a common set of disadvantages, namely, (i) limited switching speed due to considerable redistribution of minority charge carriers associated with every switching operation; (ii) relatively large control power requirement which complicates the control circuit design. Besides, bipolar devices can not be paralleled easily.

The reliance of the power electronics industry upon bipolar devices was challenged by the introduction of a new MOS gate controlled power device technology in the 1980s. The power MOS field effect transistor (MOSFET) evolved from the MOS integrated circuit technology. The new device promised extremely low input power levels and no inherent limitation to the switching speed. Thus, it opened up the possibility of increasing the operating frequency in power electronic systems resulting in reduction in size and weight. The initial claims of infinite current gain for the power MOSFET were, however, diluted by the need to design the gate drive circuit to account for the pulse currents required to charge and discharge the high input capacitance of these devices. At high frequency of operation the required gate drive power becomes substantial. MOSFETs also have comparatively higher on state resistance per unit area of the device cross section which increases with the blocking voltage rating of the device. Consequently, the use of MOSFET has been restricted to low voltage (less than about 500 volts) applications where the ON state resistance reaches acceptable values. Inherently fast switching speed of these devices can be effectively utilized to increase the switching frequency beyond several hundred kHz.

From the point of view of the operating principle a MOSFET is a voltage controlled majority carrier device. As the name suggests, movement of majority carriers in a MOSFET is controlled by the voltage applied on the control electrode (called gate) which is insulated by a thin metal oxide layer from the bulk semiconductor body. The electric field produced by the gate voltage modulate the conductivity of the semiconductor material in the region between the main current carrying terminals called the Drain (D) and the Source (S). Power MOSFETs, just like their integrated circuit counterpart, can be of two types (i) depletion type and (ii) enhancement type. Both of these can be either **n**- channel type or **p**-channel type depending on the nature of the bulk semiconductor. Fig 6.1 (a) shows the circuit symbol of these four types of MOSFETs along with their drain current vs gate-source voltage characteristics (transfer characteristics).



(a)

(b)

Fig 6.1: Different types of power MOSFET.
(a) Circuit symbols and transfer characteristics
(b) Photograph of n-channel enhancement type MOSFET.

From Fig 6.1 (a) it can be concluded that depletion type MOSFETs are normally ON type switches i.e, with the gate terminal open a nonzero drain current can flow in these devices. This is not convenient in many power electronic applications. Therefore, the enhancement type MOSFETs (particularly of the n-channel variety) is more popular for power electronics applications. This is the type of MOSFET which will be discussed in this lesson. Fig 6.1 (b) shows the photograph of some commercially available n-channel enhancement type Power MOSFETs.

6.2 Constructional Features of a Power MOSFET

As mentioned in the introduction section, Power MOSFET is a device that evolved from MOS integrated circuit technology. The first attempts to develop high voltage MOSFETs were by redesigning lateral MOSFET to increase their voltage blocking capacity. The resulting technology was called lateral double deffused MOS (DMOS). However it was soon realized that

much larger breakdown voltage and current ratings could be achieved by resorting to a vertically oriented structure. Since then, vertical DMOS (VDMOS) structure has been adapted by virtually all manufacturers of Power MOSFET. A power MOSFET using VDMOS technology has vertically oriented three layer structure of alternating **p** type and **n** type semiconductors as shown in Fig 6.2 (a) which is the schematic representation of a single MOSFET cell structure. A large number of such cells are connected in parallel (as shown in Fig 6.2 (b)) to form a complete device.

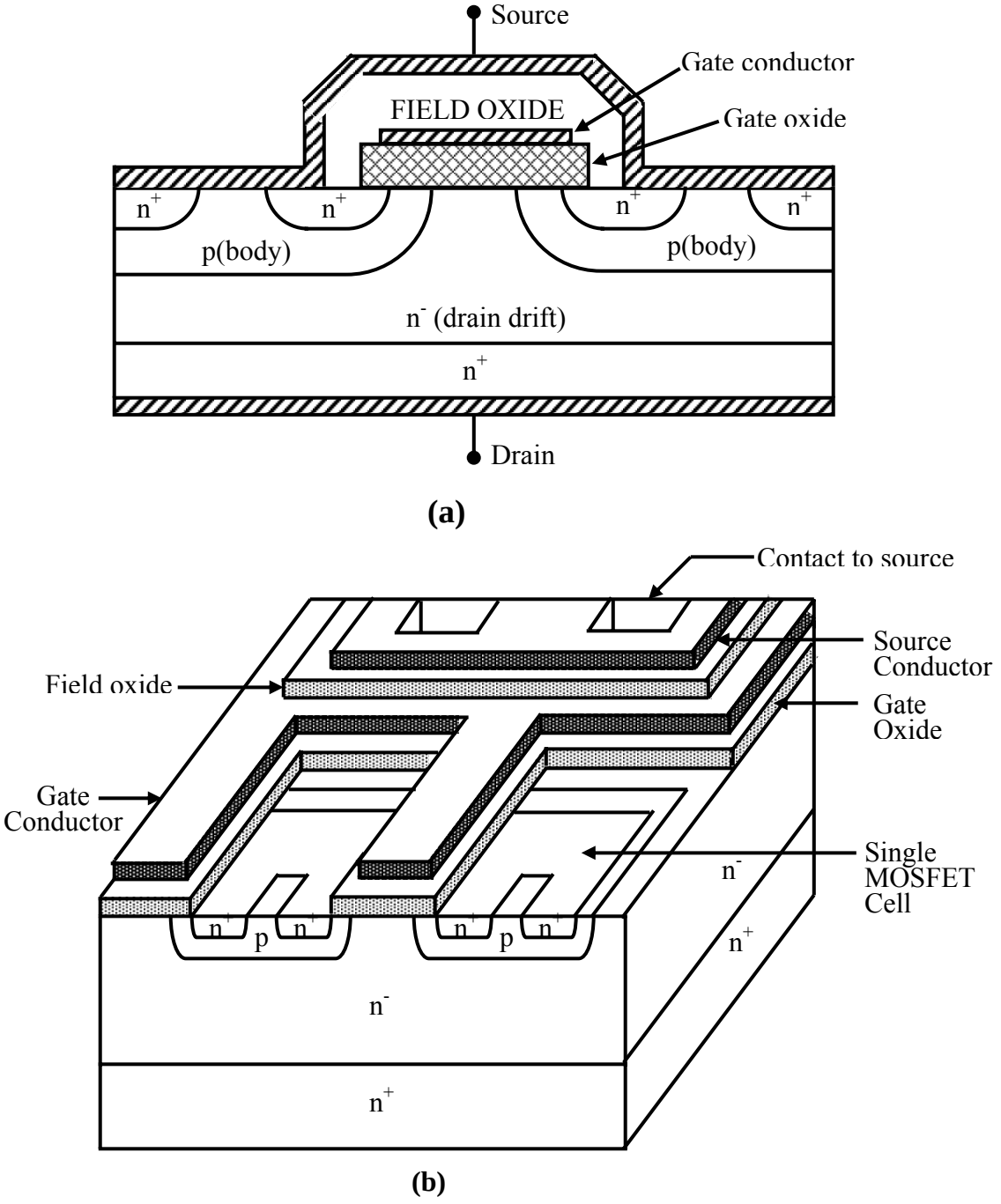


Fig. 6.2: Schematic construction of a power MOSFET
(a) Construction of a single cell.
(b) Arrangement of cells in a device.

The two $\mathbf{n^+}$ end layers labeled "Source" and "Drain" are heavily doped to approximately the same level. The **p** type middle layer is termed the body (or substrate) and has moderate doping level (2 to 3 orders of magnitude lower than $\mathbf{n^+}$ regions on both sides). The $\mathbf{n^-}$ drain drift region has the lowest doping density. Thickness of this region determines the breakdown voltage of the device. The gate terminal is placed over the $\mathbf{n^-}$ and **p** type regions of the cell structure and is insulated from the semiconductor body be a thin layer of silicon dioxide (also called the gate oxide). The source and the drain region of all cells on a wafer are connected to the same metallic contacts to form the Source and the Drain terminals of the complete device. Similarly all gate terminals are also connected together. The source is constructed of many (thousands) small polygon shaped areas that are surrounded by the gate regions. The geometric shape of the source regions, to same extent, influences the ON state resistance of the MOSFET.

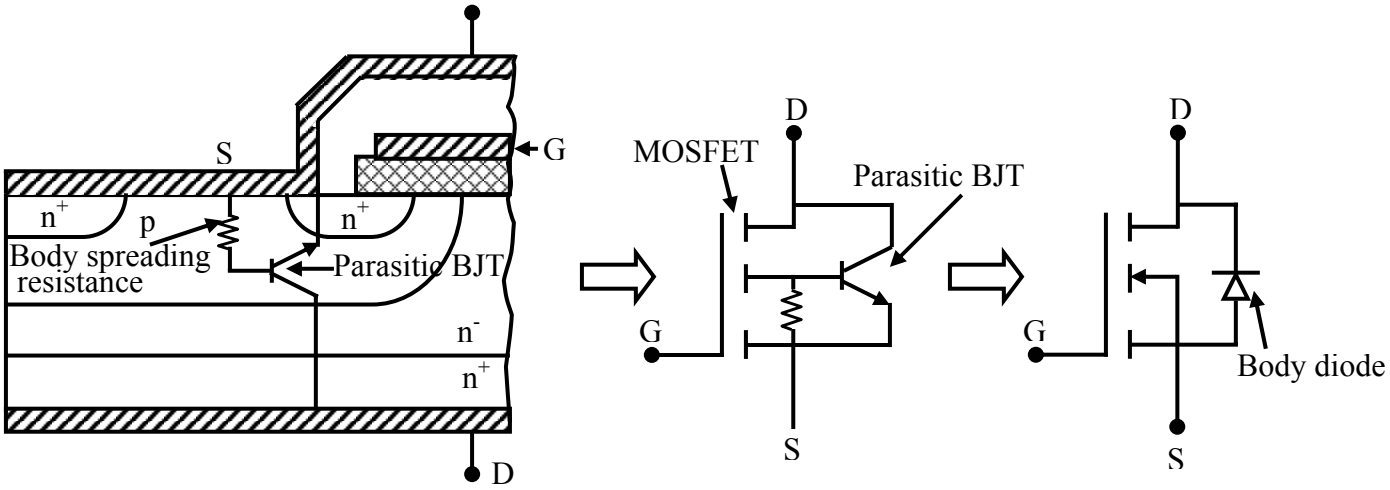


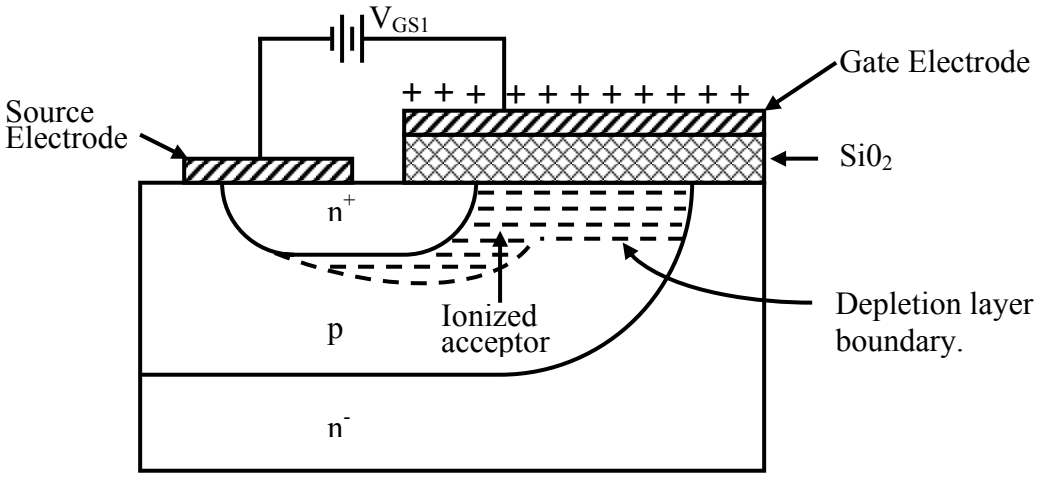
Fig. 6.3: Parasitic BJT in a MOSFET cell.

One interesting feature of the MOSFET cell is that the alternating $\mathbf{n^+}$ $\mathbf{n^-}$ **p** $\mathbf{n^+}$ structure embeds a parasitic BJT (with its base and emitter shorted by the source metallization) into each MOSFET cell as shown in Fig 6.3. The nonzero resistance between the base and the emitter of the parasitic **npn** BJT arises due to the body spreading resistance of the **p** type substrate. In the design of the MOSFET cells special care is taken so that this resistance is minimized and switching operation of the parasitic BJT is suppressed. With an effective short circuit between the body and the source the BJT always remain in cut off and its collector-base junction is represented as an anti parallel diode (called the body diode) in the circuit symbol of a Power MOSFET.

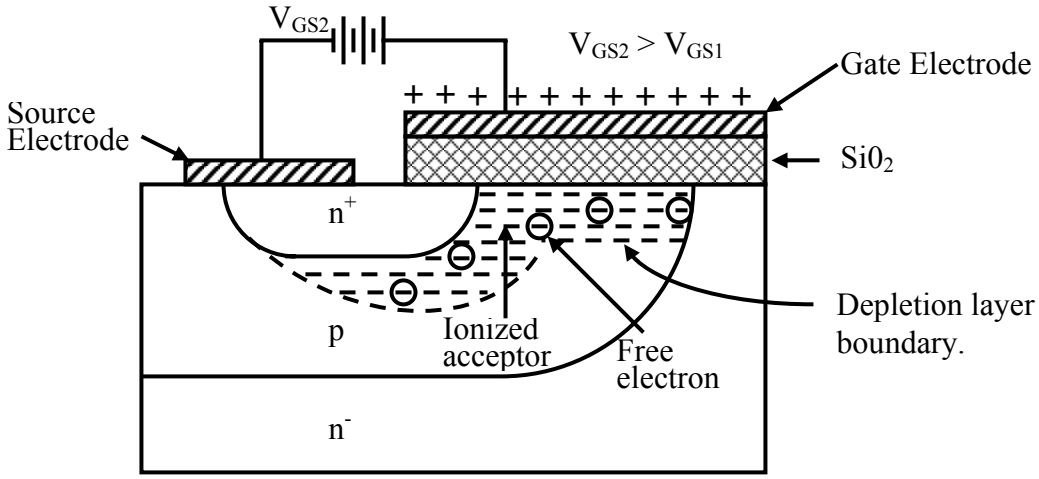
6.3 Operating principle of a MOSFET

At first glance it would appear that there is no path for any current to flow between the source and the drain terminals since at least one of the **p** **n** junctions (source – body and body-Drain) will be reverse biased for either polarity of the applied voltage between the source and the drain. There is no possibility of current injection from the gate terminal either since the gate oxide is a very good insulator. However, application of a positive voltage at the gate terminal with respect to the source will covert the silicon surface beneath the gate oxide into an **n** type layer or "channel", thus connecting the Source to the Drain as explained next.

The gate region of a MOSFET which is composed of the gate metallization, the gate (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in Fig 6.4 (a).



(a)



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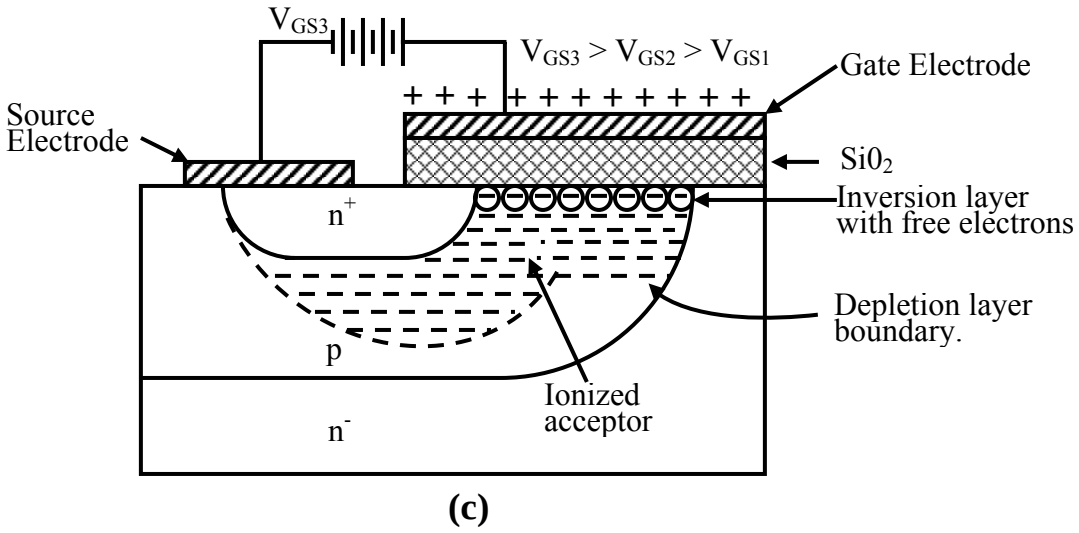

Fig. 6.4: Gate control of MOSFET conduction.
(a) Depletion layer formation;
(b) Free electron accumulation;
(c) Formation of inversion layer.

The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the **p** type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as shown in Fig 6.4 (b). The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig 6.4 (c). The inversion layer has all the properties of an **n** type semiconductor and is a conductive path or "channel" between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an **n-** type "channel" created by the electric field due to gate source voltage it is called "Enhancement type n-channel MOSFET".

The value of V_{GS} at which the inversion layer is considered to have formed is called the "Gate – Source threshold voltage V_{GS} (th)". As V_{GS} is increased beyond V_{GS}(th) the inversion layer gets some what thicker and more conductive, since the density of free electrons increases further with increase in V_{GS}. The inversion layer screens the depletion layer adjacent to it from increasing V_{GS}. The depletion layer thickness now remains constant.

Exercise 6.1 (after section 6.3)

1. Fill in the blank(s) with the appropriate word(s)

   i. A MOSFET is a _____ controlled _____ carrier device.

   ii. Enhancement type MOSFETs are normally _____devices while depletion type MOSFETs are normally _____ devices.

   iii. The Gate terminal of a MOSFET is isolated from the semiconductor by a thin layer of _____.

   iv. The MOSFET cell embeds a parasitic _____ in its structure.

   v. The gate-source voltage at which the _____ layer in a MOSFET is formed is called the _____ voltage.

   vi. The thickness of the _____ layer remains constant as gate source voltage is increased beyond the _____ voltage.

Answer: (i) voltage, majority; (ii) off, on; (iii) SiO_2, (iv) BJT, (v) inversion, threshold; (vi) depletion, threshold.

2. What are the main constructional differences between a MOSFET and a BJT? What effect do they have on the current conduction mechanism of a MOSFET?

   Answer: A MOSFET like a BJT has alternating layers of **p** and **n** type semiconductors. However, unlike BJT the **p** type body region of a MOSFET does not have an external electrical connection. The gate terminal is insulated for the semiconductor by a thin layer of SiO_2. The body itself is shorted with $\mathbf{n}^+$ type source by the source metallization. Thus minority carrier injection across the source-body interface is prevented. Conduction in a MOSFET occurs due to formation of a high density **n** type channel in the **p** type body region due to the electric field produced by the gate-source voltage. This **n** type channel connects $\mathbf{n}^+$ type source and drain regions. Current conduction takes place between the drain and the source through this channel due to flow of electrons only (majority carriers). Where as in a BJT, current conduction occurs due to minority carrier injection across the Base-Emitter junction. Thus a MOSFET is a voltage controlled majority carrier device while a BJT is a minority carrier bipolar device.

6.4 Steady state output i-v characteristics of a MOSFET

The MOSFET, like the BJT is a three terminal device where the voltage on the gate terminal controls the flow of current between the output terminals, Source and Drain. The source terminal is common between the input and the output of a MOSFET. The output characteristics of a MOSFET is then a plot of drain current (i_D) as a function of the Drain – Source voltage (v_{DS}) with gate source voltage (v_{GS}) as a parameter. Fig 6.5 (a) shows such a characteristics.

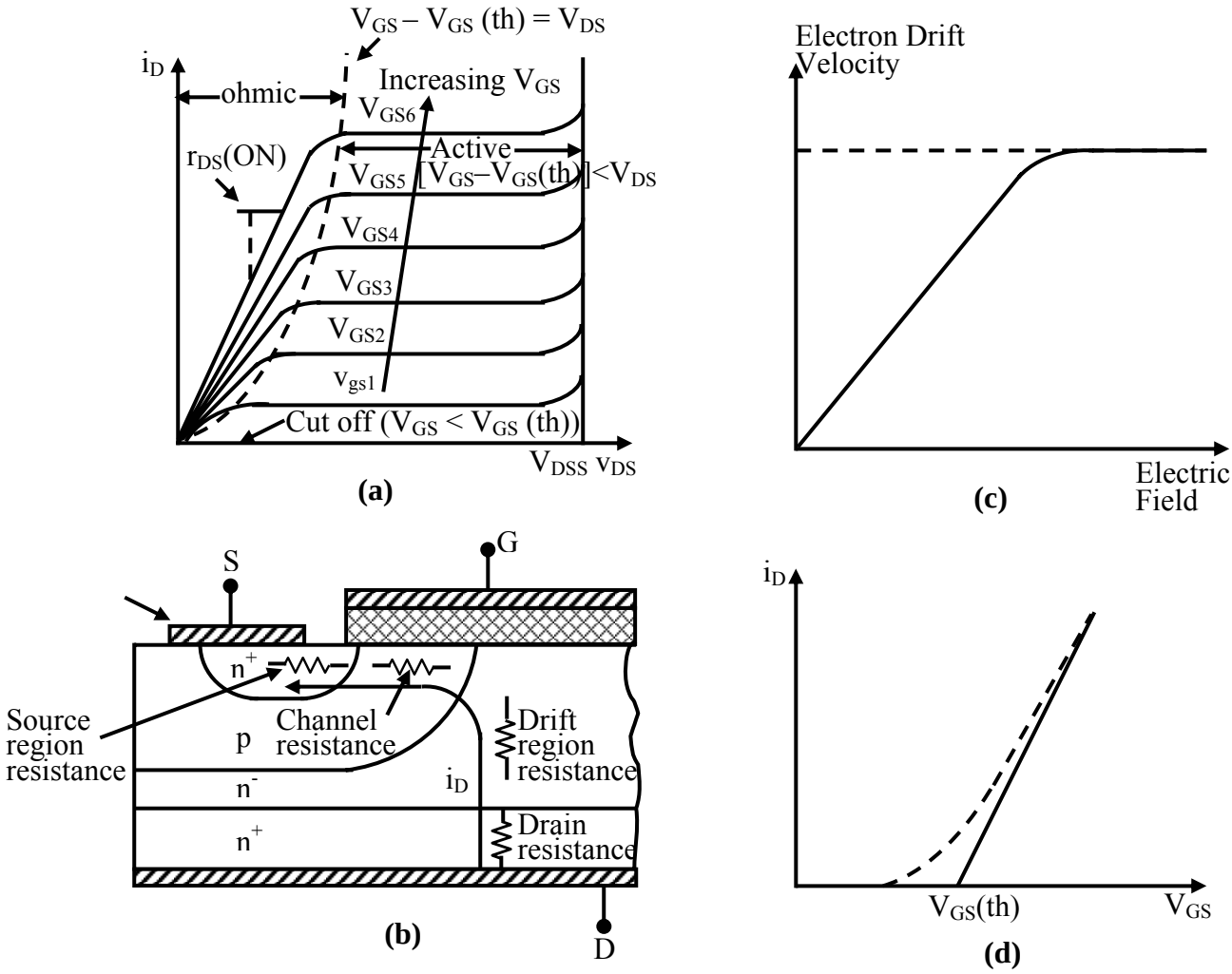

Fig. 6.5: Output i-v characteristics of a Power MOSFET
(a) i-v characteristics;
(b) Components of ON-state resistance;
(c) Electron drift velocity vs Electric field;
(d) Transfer

With gate-source voltage (V_{GS}) below the threshold voltage (v_{GS} (th)) the MOSFET operates in the cut-off mode. No drain current flows in this mode and the applied drain–source voltage (v_{DS}) is supported by the body-collector **p-n** junction. Therefore, the maximum applied voltage should be below the avalanche break down voltage of this junction (V_{DSS}) to avoid destruction of the device.

When V_{GS} is increased beyond $v_{GS}(th)$ drain current starts flowing. For small values of v_{DS} ($v_{DS} < (v_{GS} - v_{GS}(th))$ i_D is almost proportional to v_{DS}. Consequently this mode of operation is called "ohmic mode" of operation. In power electronic applications a MOSFET is operated either in the cut off or in the ohmic mode. The slope of the $v_{DS} - i_D$ characteristics in this mode is called the ON state resistance of the MOSFET (r_{DS} (ON)). Several physical resistances as shown in Fig 6.5 (b) contribute to r_{DS} (ON). Note that r_{DS} (ON) reduces with increase in v_{GS}. This is mainly due to reduction of the channel resistance at higher value of

v_{GS}. Hence, it is desirable in power electronic applications, to use as large a gate-source voltage as possible subject to the dielectric break down limit of the gate-oxide layer.

At still higher value of v_{DS} ($v_{DS} > (v_{GS} - v_{GS}(th))$ the $i_D - v_{DS}$ characteristics deviates from the linear relationship of the ohmic region and for a given v_{GS}, i_D tends to saturate with increase in v_{DS}. The exact mechanism behind this is rather complex. It will suffice to state that, at higher drain current the voltage drop across the channel resistance tends to decrease the channel width at the drain drift layer end. In addition, at large value of the electric field, produced by the large Drain – Source voltage, the drift velocity of free electrons in the channel tends to saturate as shown in Fig 6.5 (c). As a result the drain current becomes independent of V_{DS} and determined solely by the gate – source voltage v_{GS}. This is the active mode of operation of a MOSFET. Simple, first order theory predicts that in the active region the drain current is given approximately by

$$i_D = K(v_{GS} - v_{GS}(th))^2 \qquad (6.1)$$

Where K is a constant determined by the device geometry.

At the boundary between the ohmic and the active region

$$v_{DS} = v_{GS} - v_{GS}(th) \qquad (6.2)$$

$$\text{Therefore, } i_D = Kv_{DS}^2 \qquad (6.3)$$

Equation (6.3) is shown by a dotted line in Fig 6.5 (a). The relationship of Equation (6.1) applies reasonably well to logic level MOSFETs. However, for power MOSFETs the transfer characteristics (i_D vs v_{GS}) is more linear as shown in Fig 6.5 (d).

At this point the similarity of the output characteristics of a MOSFET with that of a BJT should be apparent. Both of them have three distinct modes of operation, namely, (i)cut off, (ii) active and (iii) ohmic (saturation for BJT) modes. However, there are some important differences as well.

- Unlike BJT a power MOSFET does not undergo second break down.
- The primary break down voltage of a MOSFET remains same in the cut off and in the active modes. This should be contrasted with three different break down voltages (V_{SUS}, V_{CEO} & V_{CBO}) of a BJT.
- The ON state resistance of a MOSFET in the ohmic region has positive temperature coefficient which allows paralleling of MOSFET without any special arrangement for current sharing. On the other hand, v_{CE} (sat) of a BJT has negative temperature coefficient making parallel connection of BJTs more complicated.

As in the case of a BJT the operating limits of a MOSFET are compactly represented in a Safe Operating Area (SOA) diagram as shown in Fig 6.6. As in the case of the FBSOA of a

BJT the SOA of a MOSFET is plotted on a log-log graph. On the top, the SOA is restricted by the absolute maximum permissible value of the drain current (I_{DM}) which should not be exceeded even under pulsed operating condition. To the left, operating restriction arise due to the non zero value of $r_{DS}(ON)$ corresponding to $v_{GS} = v_{GS}(Max)$. To the right, the first operating restriction is due to the limit on the maximum permissible junction temperature rise which depends on the power dissipation inside the MOSFET. This limit is different for DC (continuous) and pulsed operation of different pulse widths. As in the case of a BJT the pulsed safe operating areas are useful for shaping the switching trajectory of a MOSFET. A MOSFET does not undergo "second break down" and no corresponding operating limit appears on the SOA. The final operation limit to the extreme right of the SOA arises due to the maximum permissible drain source voltage (V_{DSS}) which is decided by the avalanche break down voltage of the drain -body **p-n** junction. This is an instantaneous limit. There is no distinction between the forward biased and the reverse biased SOAs for the MOSFET. They are identical.

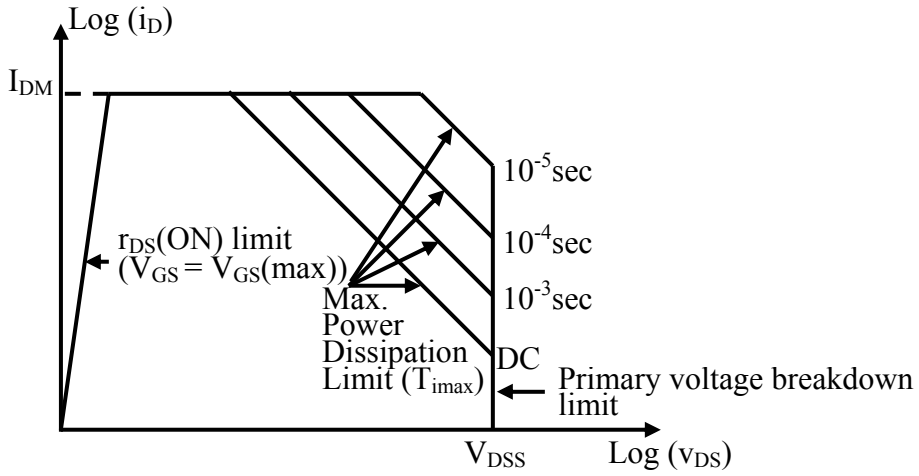

Fig. 6.6: Safe operating area of a MOSFET.

Due to the presence of the anti parallel "body diode", a MOSFET can not block any reverse voltage. The body diode, however, can carry an RMS current equal to I_{DM}. It also has a substantial surge current carrying capacity. When reverse biased it can block a voltage equal to V_{DSS}.

For safe operation of a MOSFET, the maximum limit on the gate source voltage (V_{GS} (Max)) must be observed. Exceeding this voltage limit will cause dielectric break down of the thin gate oxide layer and permanent failure of the device. It should be noted that even static charge inadvertently put on the gate oxide by careless handling may destroy it. The device user should ground himself before handling any MOSFET to avoid any static charge related problem.

Exercise 6.2

Fill in the blank(s) with the appropriate word(s)

i. A MOSFET operates in the _____ mode when $v_{GS} < v_{GS}(th)$

ii. In the ohmic region of operation of a MOSFET $v_{GS} - v_{GS}$ (th) is greater than _____.

iii. r_{DS} (ON) of a MOSFET _____ with increasing v_{GS}.

iv. In the active region of operation the drain current i_D is a function of _____ alone and is independent of _____.

v. The primary break down voltage of MOSFET is _____ of the drain current.

vi. Unlike BJT a MOSFET does not undergo _____.

vii. _____ temperature coefficient of r_{DS}(ON) of MOSFETs facilitates easy _____ of the devices.

viii. In a Power MOSFET the relation ship between i_D and $v_{GS} - v_{GS}$(th) is almost _____ in the active mode of operation.

ix. The safe operating area of a MOSFET is restricted on the left hand side by the _____ limit.

Answer: (i) Cut off; (ii) v_{DS}; (iii) decreases; (iv) v_{GS}, v_{DS}; (v) independent; (vi) second break down; (vii) Positive, paralleling; (viii) linear; (ix) r_{DS} (ON);

6.5 Switching characteristics of a MOSFET

6.5.1 Circuit models of a MOSFET cell

Like any other power semiconductor device a MOSFET is used as a switch in all power electronic converters. As a switch a MOSFET operates either in the cut off mode (switch off) or in the ohmic mode (switch on). While making transition between these two states it traverses through the active region. Being a majority carrier device the switching process in a MOSFET does not involve any inherent delay due to redistribution of minority charge carriers. However, formation of the conducting channel in a MOSFET and its disappearance require charging and discharging of the gate-source capacitance which contributes to the switching times. There are several other capacitors in a MOSFET structure which are also involved in the switching process. Unlike bipolar devices, however, these switching times can be controlled completely by the gate drive circuit design.

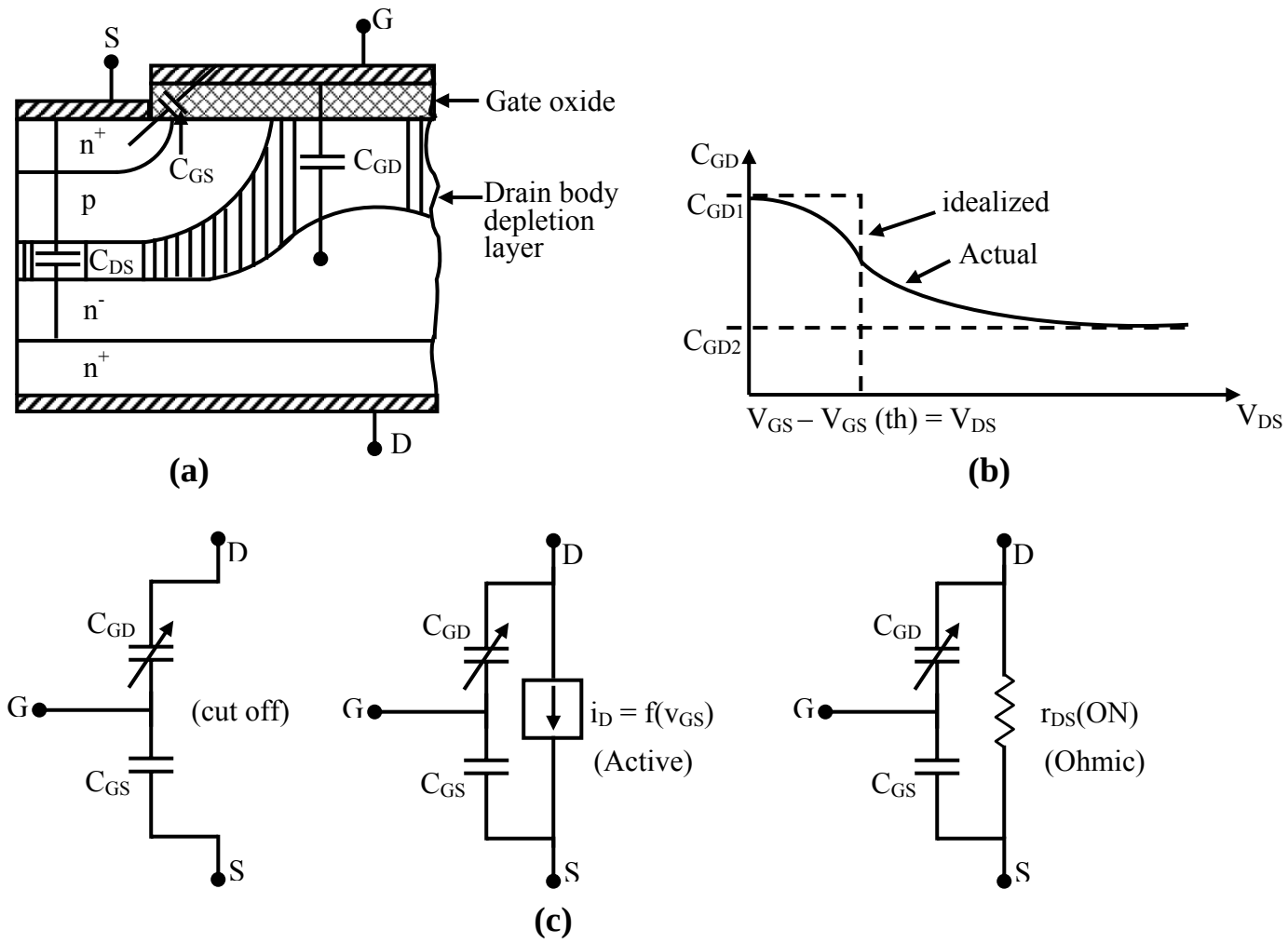

Fig. 6.7: Circuit model of a MOSFET
(a) MOSFET capacitances
(b) Variation of C_{GD} with V_{DS}
(c) Circuit models.

Fig 6.7 (a) shows three important capacitances inherent in a MOSFET structure. The most prominent capacitor in a MOSFET structure is formed by the gate oxide layer between the gate metallization and the $\mathbf{n}^+$ type source region. It has the largest value (a few nano farads) and remains more or less constant for all values of v_{GS} and v_{DS}. The next largest capacitor (a few hundred pico forwards) is formed by the drain – body depletion region directly below the gate metallization in the $\mathbf{n}^-$ drain drift region. Being a depletion layer capacitance its value is a strong function of the drain source voltage v_{DS}. For low values of v_{DS} ($v_{DS} < (v_{GS} - v_{GS}(th))$) the value of C_{GD} (C_{GD2}) is considerably higher than its value for large v_{DS} as shown in Fig 6.7 (b). Although variation of C_{GD} between C_{GD1} and C_{GD2} is continuous a step change in the value of C_{GD} at $v_{DS} = v_{GS} - v_{GS}(th)$ is assumed for simplicity. The lowest value capacitance is formed between the drain and the source terminals due to the drain – body depletion layer away form the gate metallization and below the source metallization. Although this capacitance is important for some design considerations (such as snubber design, zero voltage switching etc) it does not appreciably affect the "hard switching" performance of a MOSFET. Consequently, it will be neglected in our discussion. From the

above discussion and the steady state characteristics of a MOSFET the circuit models of a MOSFET in three modes of operation can be drawn as shown in Fig 6.7 (c).

6.5.2 Switching waveforms

The switching behavior of a MOSFET will be described in relation to the clamped inductive circuit shown in Fig 6.8. For simplicity the load current is assumed to remain constant over the small switching interval. Also the diode D_F is assumed to be ideal with no reverse recovery current. The gate is assumed to be driven by an ideal voltage source giving a step voltage between zero and V_{gg} in series with an external gate resistance R_g.

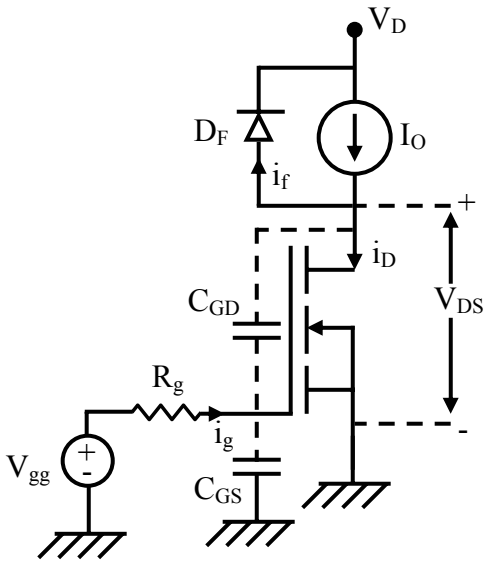

Fig. 6.8: Clamped inductive switching circuit using a MOSFET.

To turn the MOSFET on, the gate drive voltage changes from zero to V_{gg}. The gate source voltage which was initially zero starts rising towards V_{gg} with a time constant $\tau_1 = R_g (C_{GS} + C_{GD1})$ as shown in Fig 6.9.

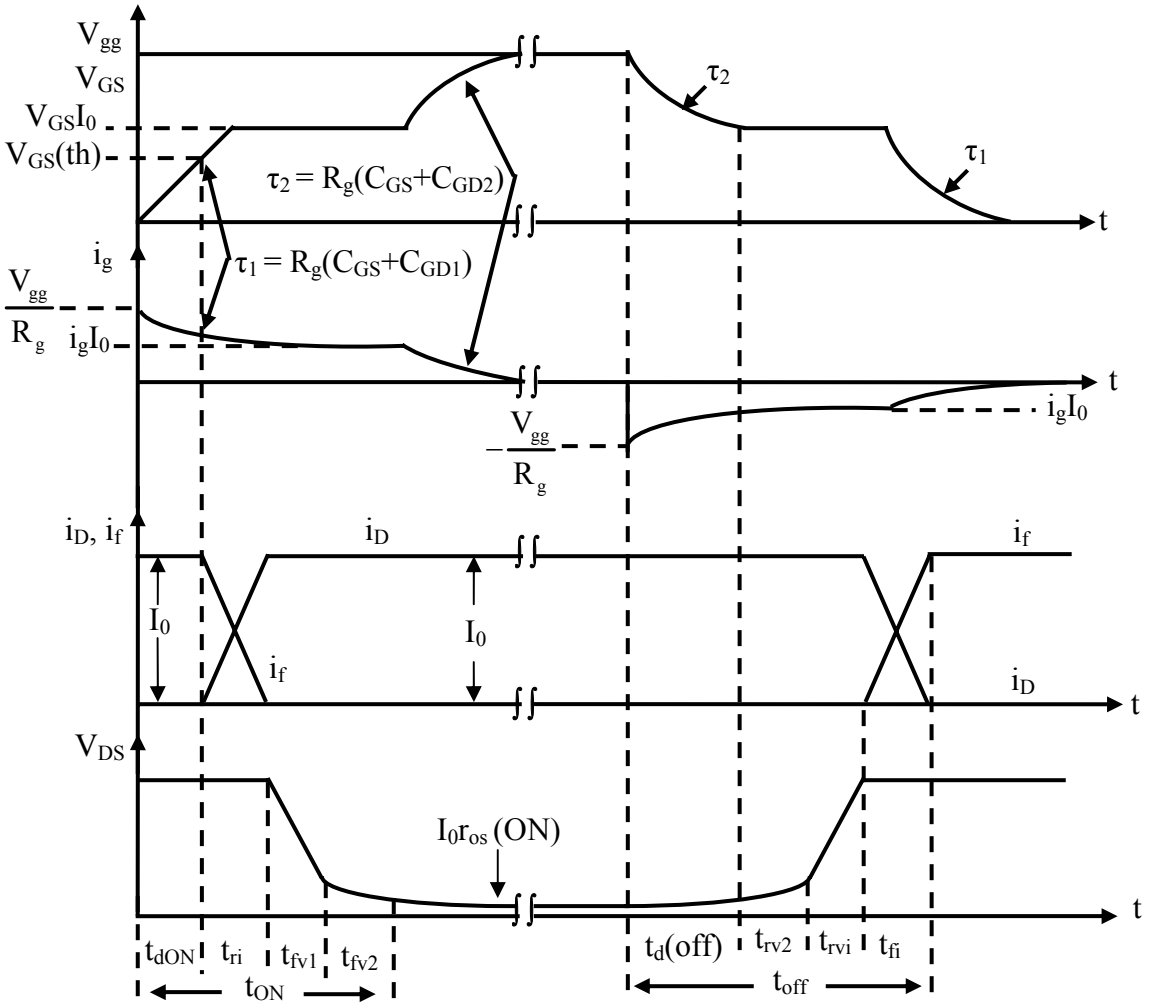

Fig. 6.9: Switching waveforms of a clamped inductive switching circuit using MOSFET

Note that during this period the drain voltage v_{DS} is clamped to the supply voltage V_D through the free wheeling diode D_F. Therefore, C_{GS} and C_{GD} can be assumed to be connected in parallel effectively. A part of the total gate current ig charges C_{GS} while the other part discharges C_{GD}.

Till v_{GS} reaches v_{GS} (th) no drain current flows. This time period is called turn on delay time (t_d(ON)). Note that t_d(ON) can be controlled by controlling R_g. Byond t_d(ON) i_D increases linearly with v_{GS} and in a further time t_{ri} (current rise time) reaches I_o. The corresponding value of v_{GS} and i_g are marked as V_{GS} I_o and i_g I_o respectively in Fig 6.9.

At this point the complete load current has been transferred to the MOSFET from the free wheeling diode D_F. i_D does not increase byond this point. Since in the active region i_D and v_{GS} are linearly related, v_{GS} also becomes clamped at the value $v_{GS}I_o$. The gate current i_g now discharges C_{GD} and the drain voltage starts falling.

$$\frac{d}{dt}v_{DS} = \frac{d}{dt}\left(v_{GS} + v_{GD}\right) = \frac{d}{dt}v_{GD} = \frac{i_g}{C_{GD}} = \frac{V_{GG} - V_{GS}I_o}{C_{GD}R_g} \qquad (6.4)$$

The fall of v_{DS} occurs in two distinct intervals. When the MOSFET is in the active region ($v_{DS} > (v_{GS} - v_{GS}(th))$ $C_{GD} = C_{GD1}$.Since $C_{GD1} << C_{GD2}$, v_{DS} falls rapidly. This fast fall time of v_{DS} is marked t_{fv1} in Fig 6.9. However, once in the ohmic region, $C_{GD} = C_{GD2} >> C_{GD1}$. Therefore, rate of fall of v_{DS} slows down considerably (t_{fv2}). Once v_{DS} reaches its on state value ($r_{DS}(ON)$ I_o) v_{GS} becomes unclamped and increases towards V_{gg} with a time constant $\tau_2 = R_g (C_{GS} + C_{GD2})$. Note that all switching periods can be reduced by increasing Vgg or / and decreasing Rg. The total turn on time is $t_{ON} = t_d(ON) + t_{ri} + t_{fv1} + t_{fv2}$.

To turn the MOSFET OFF, V_{gg} is reduced to zero triggering the exact reverse process of turn on to take place. The corresponding waveforms and switching intervals are show in Fig 6.9. The total turn off time $t_{off} = t_d(off) + t_{rv1} + t_{rv2} + t_{fi}$.

6.5.3 MOSFET Gate Drive

MOSFET, being a voltage controlled device, does not require a continuous gate current to keep it in the ON state. However, it is required to charge and discharge the gate-source and the gate-drain capacitors in each switching operation. The switching times of a MOSFET essentially depends on the charging and discharging rate of these capacitors. Therefore, if fast charging and discharging of a MOSFET is desired at fast switching frequency the gate drive power requirement may become significant. Fig 6.10 (a) shows a typical gate drive circuit of a MOSFET.

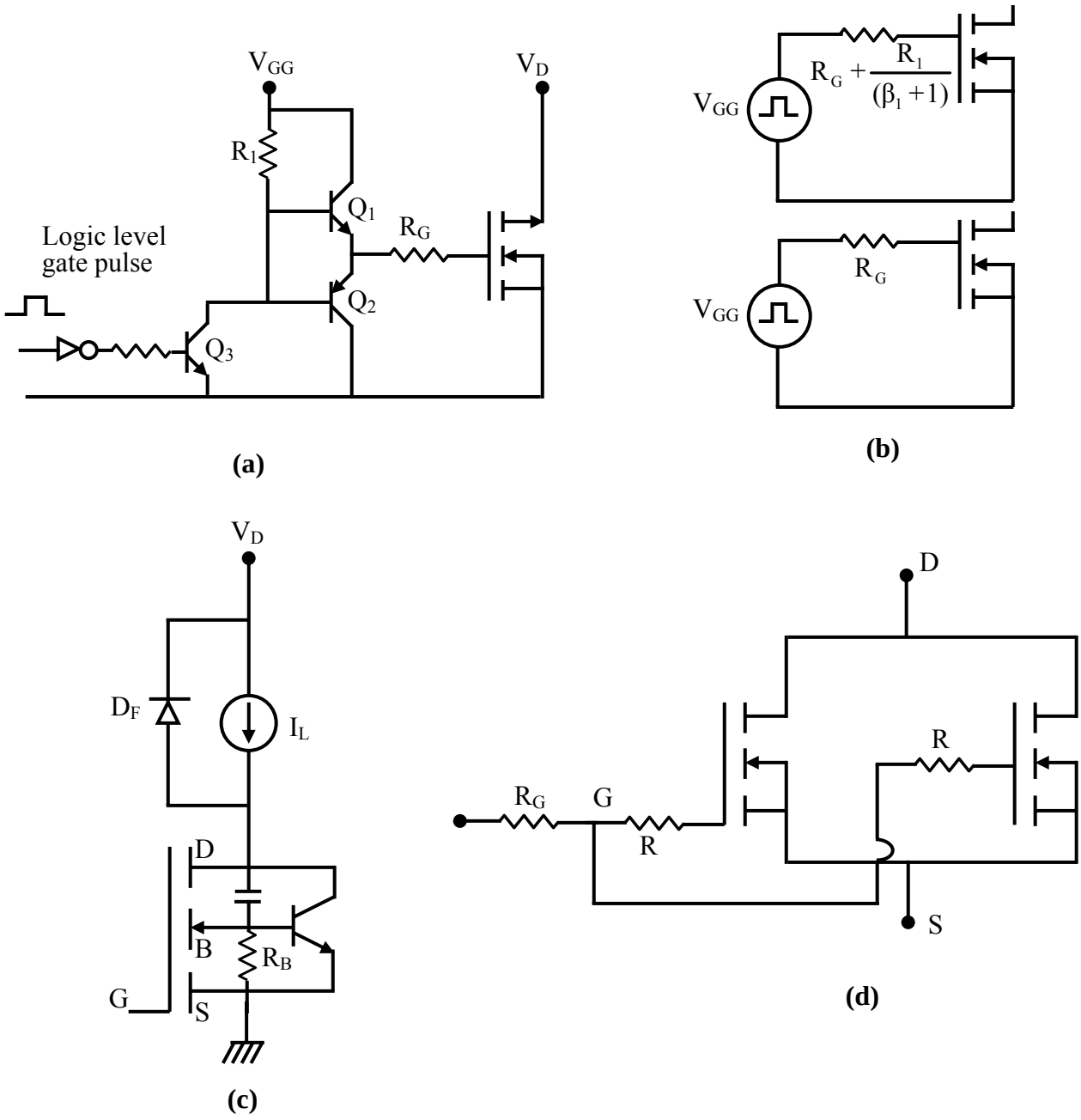

Fig. 6.10: MOSFET gate drive circuit.
(a) Gate drive circuit; (b) Equivalent circuit during turn on and off;
(b) Effect of parasitic BJT; (d) Parallel connection of MOSFET's.

To turn the MOSFET on the logic level input to the inverting buffer is set to high state so that transistor Q_3 turns off and Q_1 turns on. The top circuit of Fig 6.10 (b) shows the equivalent circuit during turn on. Note that, during turn on Q_1 remains in the active region. The effective gate resistance is $R_G + R_1 / (\beta_1 + 1)$. Where, β_1 is the dc current gain of Q_1.

To turn off the MOSFET the logic level input is set to low state. Q_3 and Q_2 turns on whole Q_1 turns off. The corresponding equivalent circuit is given by the bottom circuit of Fig 6.10 (b)

The switching time of the MOSFET can be adjusted by choosing a proper value of R_G. Reducing R_G will incase the switching speed of the MOSFET. However, caution should be exercised while increasing the switching speed of the MOSFET in order not to turn on the parasitic BJT in the MOSFET structure inadvertently. The drain-source capacitance (C_{DS}) is actually connected to the base of the parasitic BJT at the **p** type body region. The body source short has some nonzero resistance. A very fast rising drain-source voltage will send sufficient displacement current through C_{DS} and R_B as shown in Fig 6.10 (c). The voltage drop across R_B may become sufficient to turn on the parasitic BJT. This problem is largely avoided in a modern MOSFET design by increasing the effectiveness of the body-source short. The devices are now capable of dv_{DS}/dt in excess to 10,000 V/μs. Of course, this problem can also be avoided by slowing down the MOSFET switching speed.

Since MOSFET on state resistance has positive temperature coefficient they can be paralleled without taking any special precaution for equal current sharing. To parallel two MOSFETs the drain and source terminals are connected together as shown in Fig 6.10 (d). However, small resistances (R) are connected to individual gates before joining them together. This is because the gate inputs are highly capacitive with almost no losses. Some stray inductance of wiring may however be present. This stray inductance and the MOSFET capacitance can give rise to unwanted high frequency oscillation of the gate voltage that can result in puncture of the gate qxide layer due to voltage increase during oscillations. This is avoided by the damping resistance R.

Exercise 6.3

1. Fill in the blank(s) with the appropriate word(s)

   i. The Gate-Source capacitance of a MOSFET is the _____ among all three capacitances.

   ii. The Gate-Drain transfer capacitance of a MOSFET has large value in the _____ region and small value in the _____ region.

   iii. During the turn on delay time the MOSFET gate source voltage rises from zero to the _____ voltage.

   iv. The voltage fall time of a MOSFET is _____ proportional to the gate charging resistance.

   v. Unlike BJT the switching delay times in a MOSFET can be controlled by proper design of the _____ circuit.

Answer: (i) largest; (ii) ohmic, active; (iii) threshold; (iv) inversely; (v) gate drive.

2. A Power MOSFET has the following data
C_{GS} = 800 pF ; C_{GD} = 150 pF; g_f= 4; $v_{GS}(th)$ = 3V;
It is used to switch a clamped inductive load (Fig 6.8) of 20 Amps with a supply voltage V_D= 200V. The gate drive voltage is v_{gg} = 15V, and gate resistance R_g = 50Ω. Find out maximum value of $\left|\frac{di_d}{dt}\right|$ and $\left|\frac{dv_{DS}}{dt}\right|$ during turn ON.

Answer: During turn on

$$i_D \approx g_f\left(v_{gs} - v_{gs}(th)\right)$$

$$\therefore \frac{di_D}{dt} = g_f \frac{dv_{gs}}{dt}$$

But $\left(C_{GS} + C_{GD}\right)\frac{dv_{gs}}{dt} = \frac{V_{gg} - v_{gs}}{R_g}$

$$\therefore \frac{di_D}{dt} = g_f \frac{dv_{gs}}{dt} = \frac{g_f}{R_g\left(C_{GS} + C_{GD}\right)}\left(V_{gg} - v_{gs}\right)$$

$$\therefore \left|\frac{di_D}{dt}\right|_{Max} = \frac{g_f}{R_g\left(C_{GS} + C_{GD}\right)}\left(V_{gg} - v_{gs}\big|_{Min}\right) = \frac{g_f\left(V_{gg} - v_{gs}(th)\right)}{R_g\left(C_{GS} + C_{GD}\right)}$$

since for $v_{gs} < v_{gs}(th)$ $\quad i_D = \frac{di_D}{dt} = 0$

$$\therefore \left|\frac{di_D}{dt}\right|_{Max} = \frac{4}{50 \times 950 \times 10^{-12}}(15 - 3) = 1.01 \times 10^9 \text{ A/sec}$$

From equation (6.4)

$$\left|\frac{dv_{DS}}{dt}\right| = \frac{V_{gg} - V_{GS,I_o}}{C_{GD}\ R_g}$$

For I_o = 20 A, $v_{gs}(th)$ = 3V, and g_f= 4

$$V_{GS,I_o} = \frac{I_o}{g_f} + v_{gs}(th) = \frac{20}{4} + 3 = 8 \text{ volts}$$

$$\therefore \left|\frac{dv_{DS}}{dt}\right| = \frac{15 - 8}{150 \times 10^{-12} \times 50} = 933 \times 10^6 \text{ V/sec}.$$

6.6 MOSFET Ratings

Steady state operating limits of a MOSFET are usually specified compactly as a safe operating area (SOA) diagram. The following limits are specified.

V_{DSS}: This is the drain-source break down voltage. Exceeding this limit will destroy the device due to avalanche break down of the body-drain **p-n** junction.

I_{DM}: This is the maximum current that should not be exceeded even under pulsed current operating condition in order to avoid permanent damage to the bonding wires.

Continuous and Pulsed power dissipation limits: They indicate the maximum allowable value of the V_{DS}, i_D product for the pulse durations shown against each limit. Exceeding these limits will cause the junction temperature to rise beyond the acceptable limit.

All safe operating area limits are specified at a given case temperature.

In addition, several important parameters regarding the dynamic performance of the device are also specified. These are

Gate threshold voltage (V_{GS} (th)): The MOSFET remains in the cut off region when v_{GS} in below this voltage. V_{GS} (th) decreases with junction temperature.

Drain Source on state resistance (r_{DS} (ON)): This is the slope of the $i_D - v_{DS}$ characteristics in the ohmic region. Its value decreases with increasing v_{GS} and increases with junction temperature. r_{DS} (ON) determines the ON state power loss in the device.

Forward Transconductance (g_{fs}): It is the ratio of i_D and ($v_{GS} - v_{GS}$(th)). In a MOSFET switching circuit it determines the clamping voltage level of the gate – source voltage and thus influences dv_{DS}/dt during turn on and turn off.

Gate-Source breakdown voltage: Exceeding this limit will destroy the gate structure of the MOSFET due to dielectric break down of the gate oxide layer. It should be noted that this limit may by exceeded even by static charge deposition. Therefore, special precaution should be taken while handing MOSFETs.

Input, output and reverse transfer capacitances (C_{GS}, C_{DS} & C_{GD}): Value of these capacitances are specified at a given drain-source and gate-source voltage. They are useful for designing the gate drive circuit of a MOSFET.

In addition to the main MOSFET, specifications pertaining to the "body diode" are also provided. Specifications given are

Reverse break down voltage: This is same as V_{DSS}

Continuous ON state current (I_S): This is the RMS value of the continuous current that can flow through the diode.

Pulsed ON state current (I_{SM}): This is the maximum allowable RMS value of the ON state current through the diode given as a function of the pulse duration.

Forward voltage drop (v_F): Given as an instantaneous function of the diode forward current.

Reverse recovery time (t_{rr}) and Reverse recovery current (I_{rr}): These are specified as functions of the diode forward current just before reverse recovery and its decreasing slope (di_F/dt).

Exercise 6.4

Fill in the blank(s) with the appropriate word(s)

i. The maximum voltage a MOSFET can with stand is _____ of drain current.

ii. The FBSOA and RBSOA of a MOSFET are _____.

iii. The gate source threshold voltage of a MOSFET _____ with junction temperature while the on state resistance _____ with junction temperature.

iv. The gate oxide of a MOSFET can be damaged by _____ electricity.

v. The reverse break down voltage of the body diode of a MOSFET is equal to _____ while its RMS forward current rating is equal to _____.

Answer: (i) independent; (ii) identical; (iii) decreases, increases; (iv) static; (v) V_{DSS}; I_{DM}.

Reference

[1] "Evolution of MOS-Bipolar power semiconductor Technology", B. Jayant Baliga, Proceedings of the IEEE, VOL.76, No-4, April 1988.

[2] "Power Electronics ,Converters Application and Design" Third Edition, Mohan, Undeland, Robbins. John Wiley & Sons Publishers 2003.

[3] GE – Power MOSFET data sheet.

Lesson Summary

- MOSFET is a voltage controlled majority carrier device.
- A Power MOSFET has a vertical structure of alternating **p** and **n** layers.
- The main current carrying terminals of an **n** channel enhancement mode MOSFET are called the Drain and the Source and are made up of $\mathbf{n}^+$ type semiconductor.
- The control terminal is called the Gate and is isolated form the bulk semiconductor by a thin layer of SiO_2.
- **p** type semiconductor body separates $\mathbf{n}^+$ type source and drain regions.
- A conducting **n** type channel is produced in the **p** type body region when a positive voltage greater than a threshold voltage is applied at the gate.
- Current conduction in a MOSFET occurs by flow of electron from the source to the drain through this channel.
- When the gate source voltage is below threshold level a MOSFET remains in the "Cut Off" region and does not conduct any current.
- With $v_{GS} > v_{GS}$ (th) and $v_{DS} < (v_{GS} - v_{GS}$ (th)) the drain current in a MOSFET is proportional to v_{DS}. This is the "Ohmic region" of the MOSFET output characteristics.
- For larger values of v_{DS} the drain current is a function of v_{GS} alone and does not depend on v_{Ds}. This is called the "active region" of the MOSFET.
- In power electronic applications a MOSFET is operated in the "Cut Off" and Ohmic regions only.
- The on state resistance of a MOSFET (V_{DS} (ON)) has a positive temperature coefficient. Therefore, MOSFETs can be easily paralleled.
- A MOSFET does not undergo second break down.
- The safe operating area (SOA) of a MOSFET is similar to that of a BJT except that it does not have a second break down limit.
- Unlike BJT the maximum forward voltage withstanding capability of a MOSFET does not depend on the drain current.
- The safe operating area of a MOSFET does not change under Forward and Reverse bias conditions.
- The drain – body junction in a MOSFET structure constitute an anti parallel diode connected between the source and the drain. This is called the MOSFET "body – diode."
- The body diode of a MOSFET has the same break down voltage and forward current rating as the main MOSFET.
- The switching delays in a MOSFET are due to finite charging and discharging time of the input and output capacitors.
- Switching times of a MOSFET can be controlled completely by external gate drive design.

- The input capacitor along with the gate drive resistance determine the current rise and fall time of a MOSFET during switching.
- The transfer capacitor (C_{gd}) determines the drain voltage rise and fall times.
- r_{DS} (ON) of a MOSFET determines the conduction loss during ON period.
- r_{DS} (ON) reduces with higher v_{gs}. Therefore, to minimize conduction power loss maximum permissible v_{gs} should be used subject to dielectric break down of the gate oxide layer.
- The gate oxide layer can be damaged by static charge. Therefore MOSFETs should be handled only after discharging one self through proper grounding.
- For similar voltage rating, a MOSFET has a relatively higher conduction loss and lower switching loss compared to a BJT. Therefore, MOSFETs are more popular for high frequency (>50 kHz) low voltage (<100 V) circuits.

Practice Problems and Answers

Practice Problems

1. How do you expect the gate source capacitance of a MOSFET to varry with gate source voltage. Explain your answer.

2. The gate oxide layer of a MOSFET is 1000 Angstrom thick Assuming a break down field strength of 5×10^6 V/cm and a safely factor of 50%, find out the maximum allowable gate source voltage.

3. Explain why in a high voltage MOSFET switching circuit the voltage rise and fall time is always greater than current fall and rise times.

4. A MOSFET has the following parameters

   $V_{GS}(th) = 3V$, $g_{fs} = 3$, $C_{GS} = 800$ PF, $C_{GD} = 250$ PF. The MOSFET is used to switch an inductive load of 15 Amps from 150V supply. The switching frequency is 50 kHz. The gate drive circuit has a driving voltage of 15V and output resistance of 50Ω. Find out the switching loss in the MOSFET.

Answer to practice problems

1. When the gate voltage is zero the thickness of the gate-source capacitance is approximately equal to the thickness of the gate oxide layer. As the gate source voltage increases the width of the depletion layer in the **p** body region also increases. Since the depletion layer is a region of immobile charges it in effect increases the thickness of the gate-source capacitance and hence the value of this capacitances decreases with increasing v_{GS}. However, as v_{GS} is increased further free electrons generated by thermal ionization get attracted towards the gate oxide-semiconductor interface. These free electrons screen the depletion layer partially and the gate-source capacitance starts increasing again. When v_{GS} is above v_{gs} (th) the inversion layer completely screens the depletion layer and the effective thickness of the gate-source capacitance becomes once again equal to the thickness of the oxide layer. There after the value of C_{GS} remains more or less constant.

2. From the given data the break down gate source voltage

$$v_{GS}\Big|_{BD} = E_{BD} \times t_{gs}$$

where E_{BD} = Break down field strength

t_{gs} = thickness of the oxide layer.

So $v_{GS}\Big|_{BD} = 5\times10^{6}\times1000\times10^{-8} = 50\text{V}$

Let $v_{gs}\Big|_{Max}$ be the maximum allowable gate source voltage assuming 50% factor of safety.

$$\therefore \quad 1.5 \;\; v_{gs}\Big|_{Max} = v_{GS}\Big|_{BD} = 50\text{ V}$$

$$\therefore v_{gs}\Big|_{Max} = \frac{50}{1.5}\text{V} \approx 33\text{ Volts.}$$

3. We Know that for MOSFET

$$i_D = g_{fs}\left(V_{GS} - V_{GS}(th)\right)$$

$$\therefore \quad \frac{di_D}{dt} = g_{fs}\frac{d}{dt}v_{GS} = g_{fs}\frac{\left(V_{gg} - v_{GS}\right)}{R_g\ C_{GS}}$$

During current rise $V_{gg} >> v_{GS}$

$$\therefore \frac{di_D}{dt} \approx \frac{g_{fs}}{R_g C_{GS}}V_{gg}$$

$$\therefore t_{ri} = t_{fi} \approx \frac{I_o}{g_{fs}V_{gg}}\ R_g C_{GS} \quad \text{where } I_o = \text{load current.}$$

Now From equation (6.4)

$$\frac{d}{dt}v_{DS} = \frac{V_{gg} - V_{gs}, I_o}{R_g\ C_{GD}} \approx \frac{V_{gg}}{R_g\ C_{GD}}$$

Since $V_{gg} >> V_{gs}$, I_o

$$\therefore t_{rr} = t_{fv} \approx \frac{V_D}{V_{gg}} R_g C_{GD} \quad \text{where } V_D = \text{Load voltage.}$$

$$\therefore \quad \frac{t_{ri}}{t_{rr}} = \frac{t_{fi}}{t_{fr}} = \frac{I_o}{V_D} \quad \frac{C_{GS}}{g_{fs} C_{GD}}$$

That is current rise and fall times are much shorter than voltage rise and fall times.

4. Referring to Fig 6.9 energy loss during switching occurs during intervals t_{ri} , t_{fv1}, t_{fv2}, t_{rv2},t_{rv1}, and t_{fi}. For simplicity it will be assumed that $t_{fv2} = t_{rv2} = 0$. Also the rise and fall of i_D and v_{DS} will be assumed to be linear.

During t_{ri}

$$i_D = g_{fs}(v_{gs} - v_{gs}(th))$$

$$\therefore \frac{di_D}{dt} = g_{fs} \frac{d}{dt} v_{gs} = g_{fs} \frac{V_{gg} - v_{gs}}{(C_{GS} + C_{GD})R_g}$$

$$\therefore \frac{di_D}{dt} \approx \frac{g_{fs} V_{gg}}{(C_{GS} + C_{GD})R_g} \text{since} V_{gg} >> v_{gs} \text{ during current rise}$$

$$\therefore t_{ri} = \frac{I_o}{g_{fs} V_{gg}} (C_{GS} + C_{GD}) R_g$$

Energy loss during t_{ri} is

$$E_{ON1} = \frac{1}{2} t_{ri} V_D Io = \frac{V_D I_o^2}{2 g_{fs} V_{gg}} (C_{GS} + C_{GD}) R_g$$

During t_{fv}

$$\frac{dV_{DS}}{dt} = \frac{V_{gg} - V_{gs,} I_o}{C_{GD} R_g}$$

$$\text{But } V_{gs}, I_o = \frac{I_o}{g_{fs}} + v_{gs}(th)$$

$$\therefore \frac{dV_{DS}}{dt} = \frac{V_{gg} - v_{gs}(th) - I_o / g_{fs}}{R_g C_{GD}}$$

$$\therefore t_{fv} = \frac{V_D}{V_{gg} - V_{gs}(th) - I_o / g_{fs}} R_g C_{GD}$$

Energy loss during t_{fv} is

$$E_{ON2} = 1/2 \, t_{fv} I_o V_D$$

$$= \frac{V_D{}^2 I_o}{2\left(V_{gg} - v_{gs}(th) - I_o / g_{fs} \right)} R_g C_{GD}$$

$\therefore$ Energy loss during Turn on is

$$E_{ON} = E_{ON1} + E_{ON2} = \frac{V_D I_o R_g}{2}\left[\frac{I_o\left(C_{GS}+C_{GD}\right)}{g_{fs}V_{gg}} + \frac{V_D C_{GD}}{\left(V_{gg} - V_{gs}(th)\right)}\right]$$

From the symmetry of the Turn ON and the Turn OFF operation of MOSFET (i.e. $t_{ri} = t_{fi}$, $t_{fv} = t_{rv}$)

$$E_{ON} = E_{OFF}$$

$\therefore$ Total switching energy lass is $E_{sw} = E_{ON} + E_{OFF} = 2\,E_{ON}$

$$\therefore \quad E_{sw} = V_D I_o R_g C_{GD}\left[\frac{I_o/g_{fs}}{V_{gg}}\left(1+\frac{C_{GS}}{C_{GD}}\right) + \frac{VD/V_{gg}}{\frac{V_{gs}(th)}{V_{gg}} - \frac{I_o/g_{fs}}{V_{gg}}}\right]$$

$$\therefore \; P_{sw}E_{sw} = V_D I_o R_g C_{GD} f_{sw}\left[\left(1+\frac{C_{GS}}{C_{GD}}\right)\frac{I_o/g_{fs}}{V_{gg}} + \frac{VD/V_{gg}}{1-\frac{v_{gs}(th)}{V_{gg}} - \frac{I_o/g_{fs}}{v_{gg}}}\right]$$

Substituting the values given

$P_{sw} = 32$ mw,

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