LEAKAGE POWER TRENDS

Development of the digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. At 90 nm and below, leakage power management is essential in the ASIC design process. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current.

Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. At the same time power dissipation increases. To counteract increase in active and leakage power Vth should also be scaled. Leakage power is catching up with the dynamic power in VDSM CMOS circuits as shown in Figure 1.
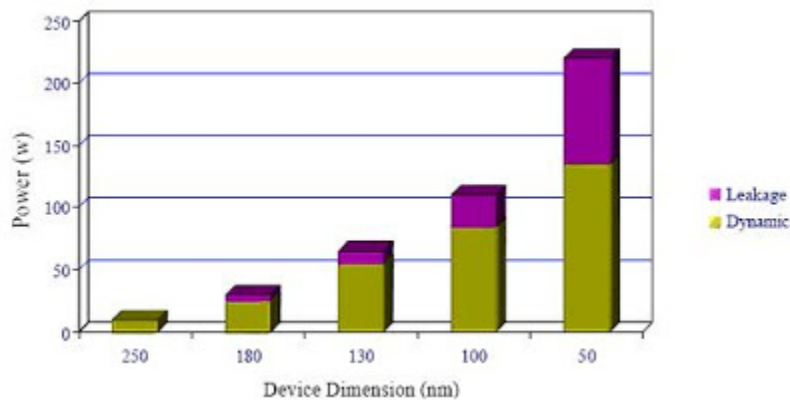

Figure 1. Leakage vs.Dynamic power [3]

According to Sung Mo Kang et al.[1] and Anantha P. Chandrakasan et al.[2] power consumption in a circuit can be divided into 3 different components. They are:

1) dynamic

2) static (or leakage) and

3) Short circuit power consumption.

Dynamic (or switching) power consumption occurs when signals which go through the CMOS circuits change their logic state charging and discharging of output node capacitor.

Leakage power consumption is the power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor.

Short circuit power consumption occurs during switching of both NMOS and PMOS transistors in the circuit and they conduct simultaneously for a short amount of time.

Leakage Power

The power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor is considered as leakage power. The leakage power of a CMOS logic gate does not depend on input transition or load capacitance and hence it remains constant for a logic cell.
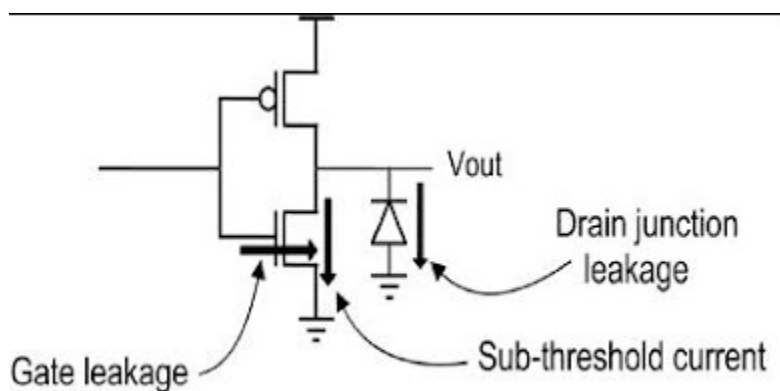

Figure 2. Leakage power components in an inverter [5]

Leakage Components in Bulk CMOS

Different leakage power components are classified are as follows and are shown in Figure 3.

- Diode reverse bias current or Reverse-biased, drain- and source-substrate junction band-to-band-tunneling (BTBT) –I1
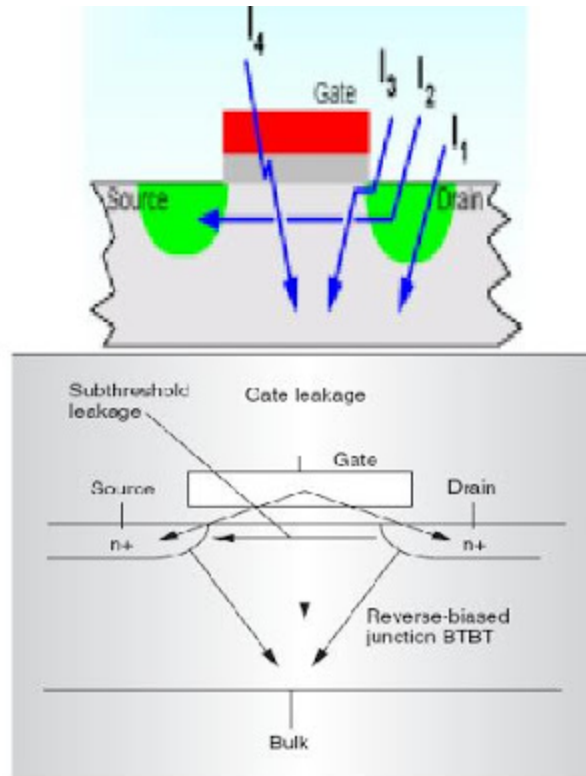- Sub threshold current – I2
- Gate induced drain leakage – I3

Figure 3. Major leakage components in a transistor [2] [3]

As technology node shrinks towards 45 nm and below gate leakage (i.e. leakage current due to direct tunneling) increases owing to the increased electric field. This is the reason why voltage is scaled down to around 1V. Improvements in the manufacturing process and material have helped to control other leakage components such as sub threshold leakage, GIDL and junction reverse bias leakage. A comparative graphical representation of different leakage currents in different technology nodes is shown in Figure 4.
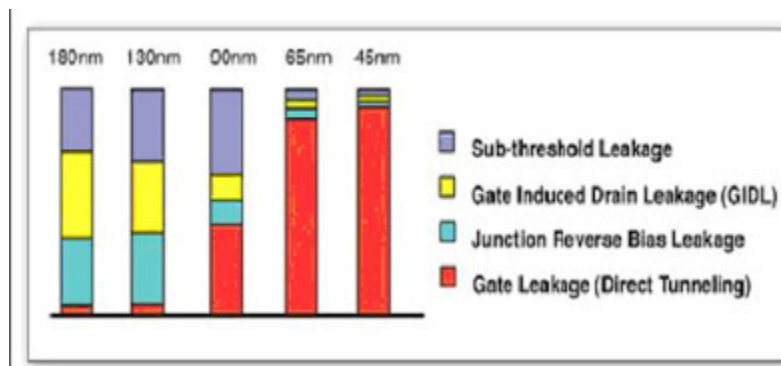
Figure 4. Technology shrinking vs. Leakage components

Sub threshold leakage is controlled by having more control over threshold voltage. Olden process technologies are causing up to 50 % of threshold voltage variation but newer technologies produce very low threshold voltage deviation, 30 mV being maximum value. Decrease in junction area and voltage automatically decreases junction reverse bias leakage and GIDL respectively. But the tunneling effect is threatening further decrease in device dimension. Reducing the GIDL, reverse bias leakage and gate leakage due to tunneling is directly related to the improvements in fabrication chemistry of the device whereas designer has a little control over threshold voltage. The other way by which a designer can have control over these leakage components is to switch off the device itself in controlled fashion! Low power techniques like "power gating" does this effectively and "back bias" technique controls threshold voltage.

Xiaodong Zhang [3] has studied impact of dynamic and leakage power as technology node reaches deep submicron level. Their summary of the result and leakage trends studied by Massoud Pedram [4] is shown below in Table 1.

	L (µm)	Tox(µm)	Isub	Igate	Ijunc
Long Channel	>1	>3	×	×	×
Short Channel	>0.18	>3	Y	×	×
Very Short Channel	>0.090	>2	Y	Y	×
Nano Scaled	<0.090	<2	Y	Y	Y

Table 1. Leakage power trends

Wide variety of techniques have been developed to address the various aspects of the power problem and to meet power specifications. These techniques include clock gating, multi-threshold (multi-Vt) voltage cells, multiple-voltage domains, substrate biasing, dynamic voltage and frequency scaling (DVFS), power gating.

Source : http://asic-soc.blogspot.in/search/label/Deep%20Sub%20Micron%20Issues