LOW LEAKAGE NANOSCALED SOURCE AND DRAIN OVER INSULATOR FINFET WITH UNDERLAP AND HIGH K DIELECTRIC

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Abstract:
In this paper a Source and drain over Insulator (SDOI) FinFET structure in which S/D regions insulated from body by buried oxide with undoped underlap and Si_3N_4 as dielectric is studied and compared with SDOI FinFET with SiO2 as dielectric. An extensive simulation study and analysis of the effect of underlaps on SDOI FinFET has been performed using the TCAD Silvaco (DevEDIT, ATLAS). The simulations have revealed that the SDOI FinFET structures with underlaps and Si3N4 as dielectric improves short channel effect significantly.

Keywords—SDOI (source and drain over Insulator); leakage current; short-channel effects (SCEs);silicon-on-insulator (SOI); DIBL, subthreshold slope S; underlap length (L_{UN}).

1. Introduction

THE miniaturization of the device dimensions has been historically used to improve the performance of bulk CMOS devices. The scaling of MOSFET dimensions has led to increased speed, high drivability, chips with increased functionality, and reduced cost [1], [2]. The era of bulk MOSFET, however, is nearing its end. The continuation of scaling of bulk MOSFET in the nanometer range (<65 nm) has become extremely difficult as the performance of bulk MOSFET is severely degraded by short channel effects (SCEs). The most important SCEs include drain-induced barrier lowering (DIBL), threshold voltage roll off problem, increase in gate leakage current, mobility degradation, etc. When the channel length shrinks, the gate control over the channel reduces due to various SCEs, such as DIBL, charge sharing, and subsurface punch through [3]. In such a scenario, the thin-film silicon-on-insulator (SOI)-based MOSFET looks set to become the next driver for CMOS scaling. SOI technology is capable of providing increased transistor speed, reduced power consumption, low leakage power, near-ideal isolation between devices, significant reduction in parasitic capacitance, and extended scalability. A significant reduction in SCEs and a steeper subthreshold slope are obtained in the thin-film SOI-based MOSFET. SOI has also become a substrate of choice for SOI-BiCMOS technology for efficient realization of system-on-chip[4,5,6]. However, the main problems associated with the SOI technology is self-heating and low breakdown voltage[7].The self heating manifests its effects in terms of degradation in reliability and in the overall performance of the device [8]For reducing self-heating effects, the use of some higher thermal conductivity materials such as amorphous carbon [10] and silicon nitride thin films [9] was proposed to replace the conventional buried oxide (BOX).However, the fabrication of such SOI devices with high thermal conductivity layers needs complicated and costlier wafer bonding techniques, and the fabrication process is not advanced enough so far. The self-heating problems have been considerably reduced by partially insulated

devices such as BOI(Body over insulator) FinFET and SDOI FinFET that uses silicon dioxide as partial BOX [11,12,23].The substrate offers heat dissipation path, thereby resulting in reduced self-heating while achieving high breakdown voltage. As the scaling is continued to nanoscale regime and equivalent distance between source and drain is decreased, the drain is more tightly coupled to channel region through gate insulator .Hence lateral electric field lines from drain reaches larger distance into the channel causing FIBL(Fringe Induced Barrier lowering)[13,14]. As the channel length of an FET is reduced, the drain potential begins to strongly influence the channel potential, leading to an inability to shut off the channel current with the gate. This closer proximity of drain to the channel give rise to higher SCE in high k MOS devices especially DIBL and subthreshold current[20]. Hence FET will have to accompanied by undoped underlap for minimizing drain potential over channel potential and thus reducing SCE [15, 17,19]. However, the series resistance (RSD) in the underlap regions is high. Hence, I_{ON} is degraded [24].By introducing high-κ spacers, the gate-fringe field is enhanced. Thus, RSD can be lowered and I_{ON} can be increased. In this paper, SDOI FinFET device with underlap and with Si_3N_4 (k=7.5) as dielectric is simulated using the 3-D device simulator Devedit and Atlas of TCAD Silvaco [22]. An advantage of SDOI FinFET with underlap and Si_3N_4 as dielectric serves following the purposes (i) dissipation of heat generated in the device as there is no insulation beneath channel(ii)improving SCEs such as DIBL, leakage current etc(iii)increase in I_{ON}. This makes further scaling of the device possible. In this device, the BOX is present beneath the channel region. The undoped underlap with $Si0_2$ and Si_3N_4 spacers have been used. The leakage current analysis of the device has shown that the SDOI FinFET device with underlap and Si_3N_4 as dielectric has lower leakage current in comparison with the SDOI FinFET device with underlap and SiO_2 as dielectric.

This paper is divided into four sections. Section 2 discusses the SDOI FinFET structure which is been constructed in DevEDIT(3D), Silvaco. Section3 shows the simulation results and discussions have been given. Section 4 gives the conclusion.

2. Device structure

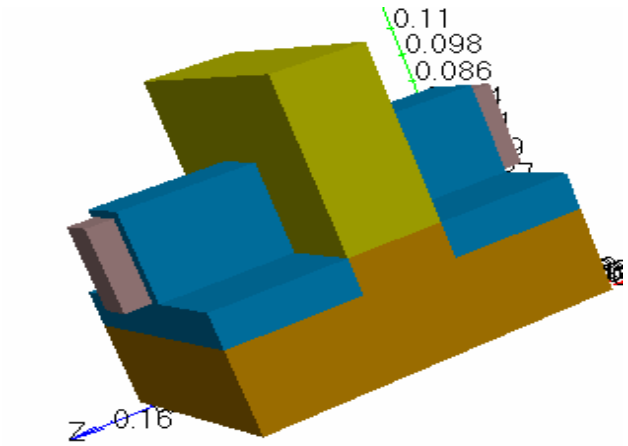

Fig1: SDOI FinFET

Fig 1 shows the insulating layer underneath the S/D region. SDOI FinFET with 30 nm gate length, 10 nm fin width and 15 nm fin height is presented. The gate oxide thickness is universally 3 nm. Polysilicon is used as gate contact and Aluminum is used for the other two terminals. In the SDOI FinFET, insulation layer of 10 nm thickness and 20 nm height is introduced underneath the S/D region.

Table1:Device dimensions(nm) and other parameters

Gate Length	**30**
Fin Height	**15**
Fin width	**10**
Gate oxide thickness	**3**
Buried layer thickness	**10**
Buried layer height	**20**
Gate material	**polysilicon**
S/D concentration	**1x10e20/cm3**
Channel Concentration	**1x10e16/cm3**

3. Simulation Results

The schematic structure of the device under condition is given in the Fig. 2. In case of the SDOI FinFET , a localized insulator is introduced at the bottom of the source and drain region which provides better heat dissipation path. Complete 3D simulations of the devices were performed using Silvaco DevEDIT (3D), Atlas TCAD software. A self-consistent Schrodinger-Poisson with Bohm Quantum Potential model (BQP) [22] is used for the simulations. The various models used in this study are fldmob, hcte, srh, fermi and bqp. The mobility model fldmob specifies that parallel electric field is used. The conventional drift-diffusion model of charge transport neglects non-local effects, such as velocity overshoot and reduced energy dependent impact ionization. These effects are incorporated in this study by using an energy balance model, which uses a higher order approximation of the Boltzmann Transport Equation. Since recombination effects are important, therefore, the concentration dependent Shockley–Read–Hall model (consrh) and Auger recombination model (auger) are activated in simulations. Similarly, we used Fermi-Dirac statistics for the simulation.

3.1 Short Channel Effects (SCEs)

The silicon fin thickness, gate oxide thickness, BOX thickness, junction depth, and channel length are the important parts of the device from an electrostatic point of view to control threshold voltage roll-off, DIBL, and subthreshold swing. The main SCEs are the threshold voltage roll-off due to charge sharing, the degradation of subthreshold swing(S), and the Drain induced barrier lowering(DIBL). These effects result in an increase in the OFF current (I_{OFF}), decrease in threshold voltage (Vth) and the deterioration of the ON–OFF current ratio (I_{ON}/ I_{OFF}). Electrostatic integrity relates both DIBL and threshold voltage roll-off SCE and describes the quality of electrostatic control of the channel by the gate.

3.2. Subthreshold Swing(S)

The subthreshold swing indicates how fast a device can react to a changing voltage level. This parameter is very important in gauging the speed of a device. Here, the variation of subthreshold swing of the simulated device against the underlap length is presented in

fig-3. Subthreshold swing is calculated from I_D-V_{GS} plot by,

Subthreshold Swing=ΔV_G (mV)/Δlog I_D (decades) (1)

Where ΔV_G is change in gate voltage,Δ I_D is change in drain current.

Subthreshold Swing S is found to be reduced by 5.6% at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET.

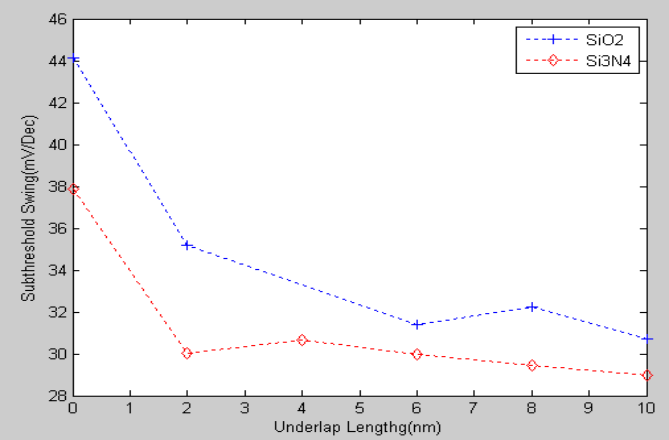

Fig 3:Effect of variation of underlap length on Subthreshold swing(S)

3.3. Threshold Voltage (Vth)

The continuation of scaling of bulk MOSFET in the nanometer range (<65 nm) has become extremely difficult as the performance of bulk MOSFET is severely degraded by short channel effects which includes threshold voltage roll off problem. As the underlap length increases control of drain over channel reduces resulting increase in threshold voltage. The variation of threshold voltage (Vth) with a change in underlap length is shown in Fig.4.Threshold voltage is found to be same at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET. But in both the cases threshold voltage is increases with increase in underlap length. Hence problem of threshold voltage roll off can be resolved by increasing underlap length. The required threshold voltage can be set by changing underlap Length.

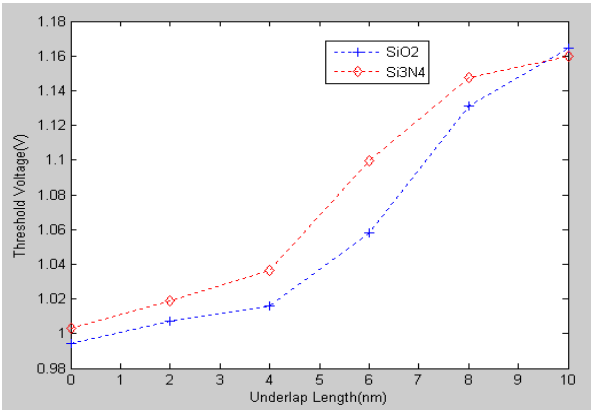

Fig4: Effect of underlap in BOI FinFET on threshold voltage (Vth)

3.4 . Leakage Current (I_{OFF})

The model for the subthreshold drain leakage current (V_{GS} = 0) is given by [6], [7], [27]

$I_{OFF} = \mu C_G (W/L)(m-1) [k_BT/q]2 \exp[-qV_T/mK_BT]$ (3)

where m is the ideality factor, which can be expressed as

$m = 1 + \gamma (C/C_G)$ (4)

Where C_G is the gate-to-channel capacitance, C represents the Channel-to-bulk capacitance.

Leakage current in the device increases the power dissipation unnecessarily and degrading the device lifetime. It is found that leakage current is found to be reduced by 44% at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET as shown in fig 5.

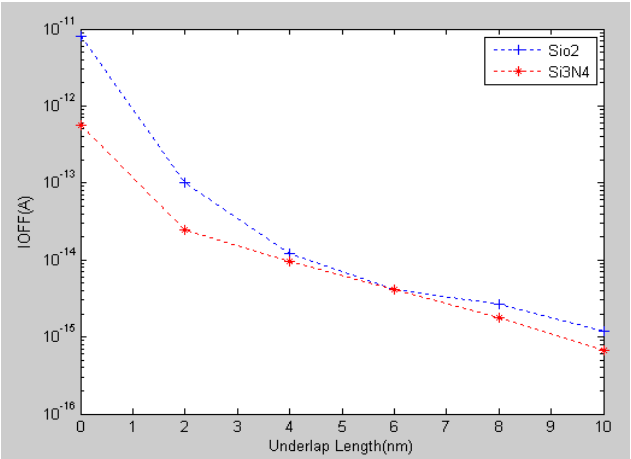

Fig5: Effect of variation of underlap length on I_{OFF}

3.5. DIBL

The fundamental electrical limitation in VLSI will be the spacing of the surface diffusions that form p-n junctions. Reverse bias on one diffused junction creates a field pattern that can lower the potential barrier separating it from an adjacent diffused junction. When this barrier lowering is large enough, the adjacent diffusion behaves as a source, resulting in an unwanted current path. But in SDOI FinFET with increased underlap length DIBL is found to be reduced by 11.43% at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET as shown in fig- 6.

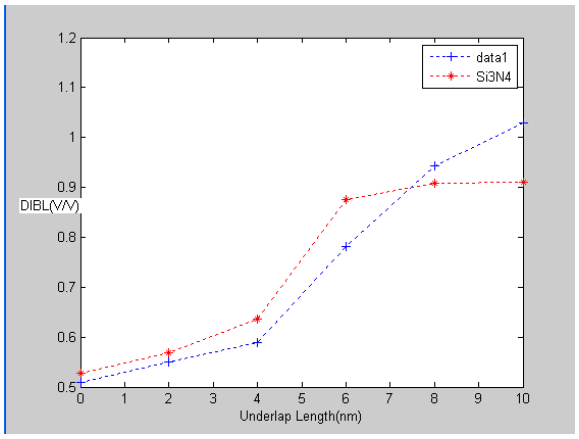

Fig 6:Effect of variation of underlap length on DIBL

3.6. Drain Current (I_{ON})

Drain current I_{ON} is found to be increased by 34% at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET.

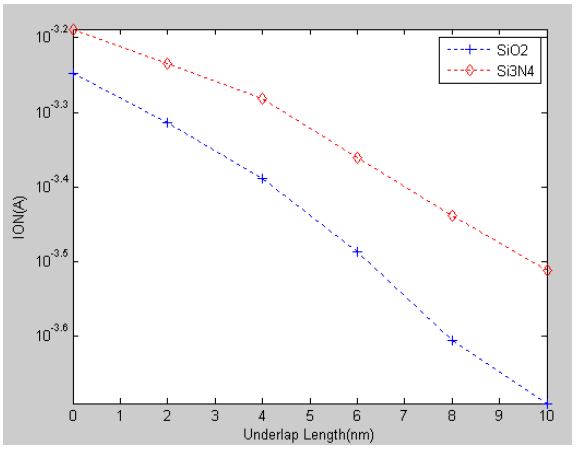

Fig7: Effect of variation of underlap length on I_{ON}

3.7 I_{ON}/I_{OFF}

The ratio I_{ON}/I_{OFF} is found to be increased by 76.7% at L_{UN} =10nm when Si_3N_4 is used as dielectric as compare to SiO_2 in SDOI FinFET as shown in fig-8.

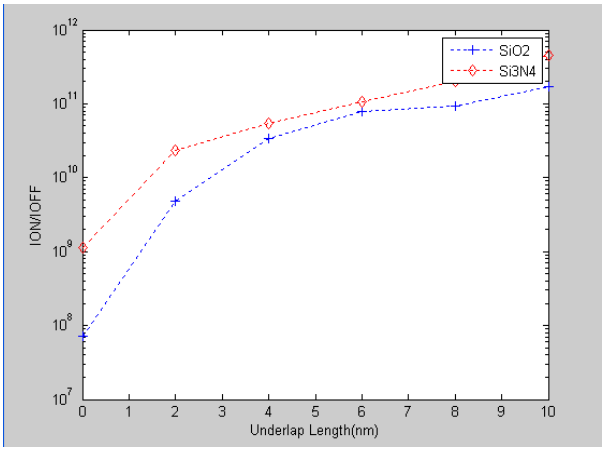

Fig8: Effect of variation of underlap length on I_{ON}/I_{OFF}

4. Conclusion

A 3-D simulation of SDOI FinFET device with underlap and spacers of SiO_2 and Si_3N_4 has been performed. The incorporation of underlap with SDOI FinFET device and with Si_3N_4 as dielectric has resulted in a significant improvement in SCEs i.e. DIBL reduces by 11.43%, leakage current reduces by 44% and I_{ON}/I_{OFF} increases by 76.7% when Si_3N_4 is used in place of SiO_2 as spacers. The use of Si_3N_4 instead of SiO_2 increases I_{ON} by 34%. The reduction in leakage current reduces power dissipation. This avoids heating, increases lifetime and ultimately the reliability of the device.

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