ELECTRICAL INTERFACE CONTROL DRAWING

Wi.Freestar Module

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1 SCOPE

THIS DRAWING DESCRIBES THE ELECTRICAL INTERFACES ASSOCIATED WITH THE WI.FREESTAR MODULE.

2 REVISION CONTROL

DATE	CHANGES	REVISION
05/13/05	INITIAL DRAFT	0.0
5/13/05	INITIAL DRAFT CORRECTIONS	0.1
8/15/05	CHANGE PORT A PIN 7 DESCRIPTION FOR WAKE UP ON INTERRUPT	0.2
10/19/05	CORRECT RXD AND TXD I/O DESCRIPTION	0.3

3 APPLICABLE DOCUMENTS

NO REFERENCED DOCUMENTS

4 TOP LEVEL BLOCK DIAGRAM

TO BE DRAWN

5 PIN DEFINTIONS

PIN	TYPE	SIGNAL NAME			ELECTRICAL DESCRIPTION
ANT2	AO/AI	ANT2			INTEGRATED PBC F-ANTENNA
TPRF1	AO/AI	TPRF1			COAXIAL RF TEST POINT – 50 OHMS
1	GND	GND			GROUND
2	GND	GND			GROUND
3	GND	GND			GROUND
4	GND	GND			GROUND
5	DI/DO	PTD3			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE, PORT D , BIT 3
6	DI/DO	PTD4			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE, PORT D , BIT 4
7	AI	PTB0			ANALOG TO DIGITAL CONVERTER INPUT, PORT B , INPUT 0
8	AI	PTB1			ANALOG TO DIGITAL CONVERTER INPUT, PORT B , INPUT 1
9	PI	VCC			PRIMARY POWER INPUT: VCC = 2.7 TO 3.6 VDC, TBD mA MAX.
10	GND	GND			GROUND
11	DI	MODE0			FCC / PRODUCTION TEST MODE INPUT WORD, BIT 0
12	DI	MODE1			FCC / PRODUCTION TEST MODE INPUT WORD, BIT 1
13	DI	MODE2			FCC / PRODUCTION TEST MODE INPUT WORD, BIT 2
14	DI/DO	PTA4			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE PORT A, BIT 4, KBI1P4 (KEYBOARD INTERRUPT)
15	DI/DO	PTA5			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE PORT A, BIT 5, KBI1P5 (KEYBOARD INTERRUPT)

PIN	TYPE	SIGNAL NAME			ELECTRICAL DESCRIPTION
16	DI/DO	PTA6			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE PORT A, BIT 6, KBI1P6 (KEYBOARD INTERRUPT)
17	DI	PTA7			DIGITAL INPUT CONFIGURED TO INTERRUPT ON RISING EDGE OF SIGNAL TO WAKE UP MODULE FROM SLEEP MODE. PORT A, BIT 7, KBI1P7 (KEYBOARD INTERRUPT)
18	DI/DO	PTGO			PORT G, BIT 0, BKGD/MS (BACKGROUND/MODE SELECT, FOR PROGRAMMING AND FIRMWARE DEBUG
19	DI	/RESET			MASTER RESET, ACTIVE LOW
20	DI/DO	PTC0			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE PORT C, BIT 0, SCI2 TXD2 (SERIAL COMMUNICATION INTERFACE 2, TRANSMIT DATA)
21	DI/DO	PTC1			GENERAL PURPOSE DIGITAL I/O FIRMWARE CONFIGURABLE PORT C, BIT 1, SCI2 RXD2 (SERIAL COMMUNICATION INTERFACE 2, RECEIVE DATA)
22	DI/DO	PTC5			RESERVED
23	DO	TXD			APPLICATION TRANSMIT DATA OUTPUT (SCI1, TXD1)
24	DI	RXD			APPLICATION RECEIVE DATA INPUT (SCI1, RXD1)
25	GND	GND			GROUND
26	GND	GND			GROUND
27	GND	GND			GROUND
28	GND	GND			GROUND
29	GND	GND			GROUND
30	GND	GND			GROUND

LEGEND:

DI = DIGITAL INPUT

DO=DIGITAL OUTPUT

AI=ANALOG INPUT

AO = ANALOG OUTPUT

PI = POWER INPUT

GND = GROUND

LOGIC INPUT HIGH: $0.8\ (V_{CC}) < V_{IH} < (V_{CC})$

LOGIC INPUT LOW: $0 < V_{IL} < 0.2\ (V_{CC})$

LOGIC OUTPUT HIGH: $(V_{CC} - 0.4) < V_{OH} < V_{CC}$

LOGIC OUTPUT LOW: $0 < V_{OH} < 0.4$

6 CONNECTOR CONFIGURATION

Note that PIN Numbering begins at top left-hand side with pin number 1 and follows counter-clockwise about the perimeter of the module.