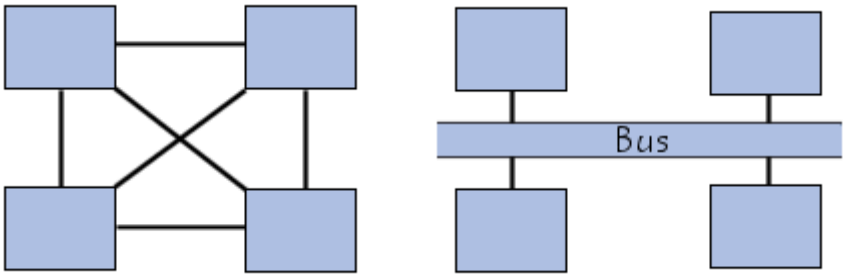
Computer bus - What is it?

Definition

A **bus**, in computing, is a set of physical connections (cables, printed circuits, etc.) which can be shared by multiple hardware components in order to communicate with one another.
The purpose of buses is to reduce the number of "pathways" needed for communication between the components, by carrying out all communications over a single data channel. This is why the metaphor of a "data highway" is sometimes used.



If only two hardware components communicate over the line, it is called a**hardware port** (such as a serial port or parallel port).

Characteristics

A bus is characterised by the amount of information that can be transmitted at once. This amount, expressed in bits, corresponds to the number of physical lines over which data is sent simultaneously. A 32-wire ribbon cable can transmit 32 bits in parallel. The term "**width**" is used to refer to the number of bits that a bus can transmit at once.

Additionally, the bus speed is also defined by its **frequency** (expressed in Hertz), the number of data packets sent or received per second. Each time that data is sent or received is called a **cycle**.

This way, it is possible to find the maximum **transfer speed** of the bus, the amount of data which it can transport per unit of time, by multiplying its width by its frequency. A

bus with a width of 16 bits and a frequency of 133 MHz, therefore, has a transfer speed equal to:

$16 * 133.10^6 = 2128*10^6$ bit/s,
or $2128*10^6/8 = 266*10^6$ bytes/s
or $266*10^6 /1000 = 266*10^3$ KB/s
or $259.7*10^3 /1000 = 266$ MB/s

Architecture

In reality, each bus is generally constituted of 50 to 100 distinct physical lines, divided into three subassemblies:

- The **address bus** (sometimes called the *memory bus*) transports memory addresses which the processor wants to access in order to read or write data. It is a unidirectional bus.
- The **data bus** transfers instructions coming from or going to the processor. It is a bidirectional bus.
- The **control bus** (or *command bus*) transports orders and synchonisation signals coming from the control unit and travelling to all other hardware components. It is a bidirectional bus, as it also transmits response signals from the hardware.

The primary buses

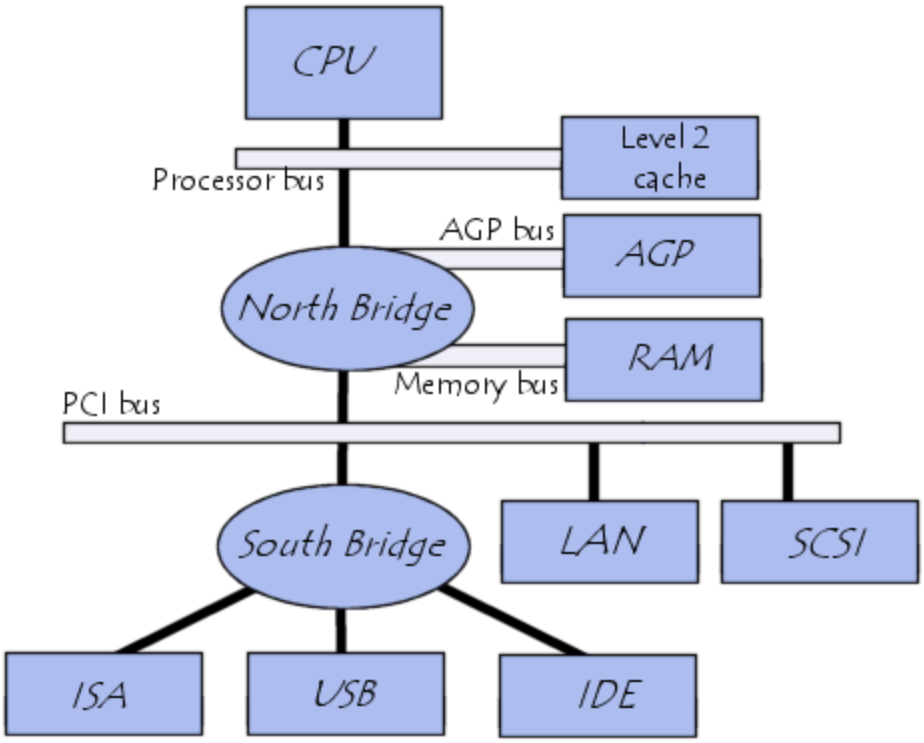
There are generally two buses within a computer:

- the **internal bus** (sometimes called the *front-side bus*, or *FSB* for short). The internal bus allows the processor to communicate with the system's central memory (the RAM).
- **the expansion bus** (sometimes called the *input/output bus*) allows variousmotherboard components (USB, serial, and parallel ports, cards inserted inPCI connectors, hard drives, CD-ROM and CD-RW drives, etc.) to communicate with one another. However, it is mainly used to add new devices using what are called **expansion slots** connected to the input/outpur bus.

Chipset

A **chipset** is the component which routes data between the computer's buses, so that all the components which make up the computer can communicate with each other. The **chipset** originally was made up of a large number of electronic chips, hence the name. It generally has two components:

- The **NorthBridge** (also called the *memory controller*) is in charge of controlling transfers between the processor and the RAM, which is way it is located physically near the processor. It is sometimes called the **GMCH**, forr *Graphic and Memory Controller Hub*.
- The **SouthBridge** (also called the *input/output controller* or *expansion controller*) handles communications between peripheral devices. It is also called the **ICH** (*I/O Controller Hub*). The tem **bridge** is generally used to designate a component which connects two buses.



It is interesting to note that, in order to communicate, two buses must have the same width. The explains why RAM modules sometimes have to be installed in pairs (for

example, early Pentium chips, whose processor buses were 64-bit, required two memory modules each 32 bits wide).
Here is a table which gives the specifications for the most commonly used buses:

Standard	Bus width (bits)	Bus speed (MHz)	Bandwidth (MB/sec)
ISA 8-bit	8	8.3	7.9
ISA 16-bit	16	8.3	15.9
EISA	32	8.3	31.8
VLB	32	33	127.2
PCI 32-bit	32	33	127.2
PCI 64-bit 2.1	64	66	508.6
AGP	32	66	254.3
AGP (x2 Mode)	32	66x2	528
AGP (x4 Mode)	32	66x4	1056
AGP (x8 Mode)	32	66x8	2112
ATA33	16	33	33
ATA100	16	50	100
ATA133	16	66	133
Serial ATA (S-ATA)	1		180
Serial ATA II (S-ATA2)	2		380
USB	1		1.5
USB 2.0	1		60
FireWire	1		100
FireWire 2	1		200
SCSI-1	8	4.77	5
SCSI-2 - Fast	8	10	10
SCSI-2 - Wide	16	10	20
SCSI-2 - Fast Wide 32 bits	32	10	40

SCSI-3 - Ultra	8	20	20
SCSI-3 - Ultra Wide	16	20	40
SCSI-3 - Ultra 2	8	40	40
SCSI-3 - Ultra 2 Wide	16	40	80
SCSI-3 - Ultra 160 (Ultra 3)	16	80	160
SCSI-3 - Ultra 320 (Ultra 4)	16	80 DDR	320
SCSI-3 - Ultra 640 (Ultra 5)	16	80 QDR	640

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