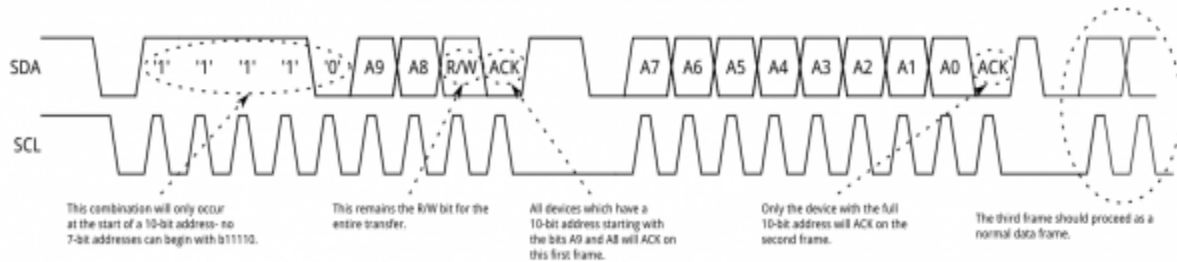


ADVANCED PROTOCOLS

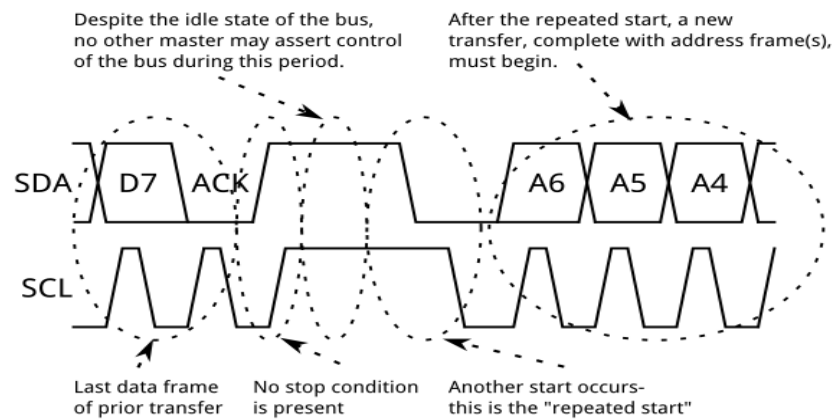
10-bit Addresses



In a 10-bit addressing system, two frames are required to transmit the slave address. The first frame will consist of the code b11110xyz, where 'x' is the MSB of the slave address, y is bit 8 of the slave address, and z is the read/write bit as described above. The first frame's ACK bit will be asserted by all slaves which match the first two bits of the address. As with a normal 7-bit transfer, another transfer begins immediately, and this transfer contains bits 7:0 of the address. At this point, the addressed slave should respond with an ACK bit. If it doesn't, the failure mode is the same as a 7-bit system.

Note that 10-bit address devices can coexist with 7-bit address devices, since the leading '11110' part of the address is not a part of any valid 7-bit addresses.

Repeated Start Conditions

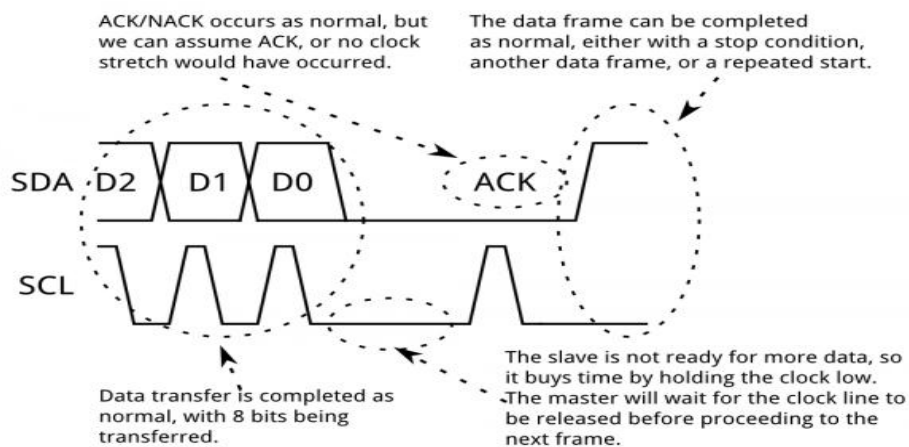


Sometimes, it is important that a master device be allowed to exchange several messages in one go, without allowing other master devices on the bus to interfere. For this reason, the repeated start condition has been defined.

To perform a repeated start, SDA is allowed to go high while SCL is low, SCL is allowed to go high, and then SDA is brought low again while SCL is high. Because there was no stop condition on the bus, the previous communication wasn't truly completed and the current master maintains control of the bus.

At this point, the next message can begin transmission. The syntax of this new message is the same as any other message—an address frame followed by data frames. Any number of repeated starts is allowed, and the master will maintain control of the bus until it issues a stop condition.

Clock stretching



At times, the master's data rate will exceed the slave's ability to provide that data.

This can be because the data isn't ready yet (for instance, the slave hasn't completed an analog-to-digital conversion yet) or because a previous operation hasn't yet completed (say, an EEPROM which hasn't completed writing to non-volatile memory yet and needs to finish that before it can service other requests).

In this case, some slave devices will execute what is referred to as "clock stretching". Nominally, **all** clocking is driven by the master device—slaves simply put data on the bus or take data off the bus in response to the master's clock pulses. At any point in the data transfer process, an addressed slave can hold the SCL line low after the master releases it. The master is required to refrain from additional clock pulses or data transfer until such time as the slave releases the SCL line.

Source: <https://learn.sparkfun.com/tutorials/i2c>