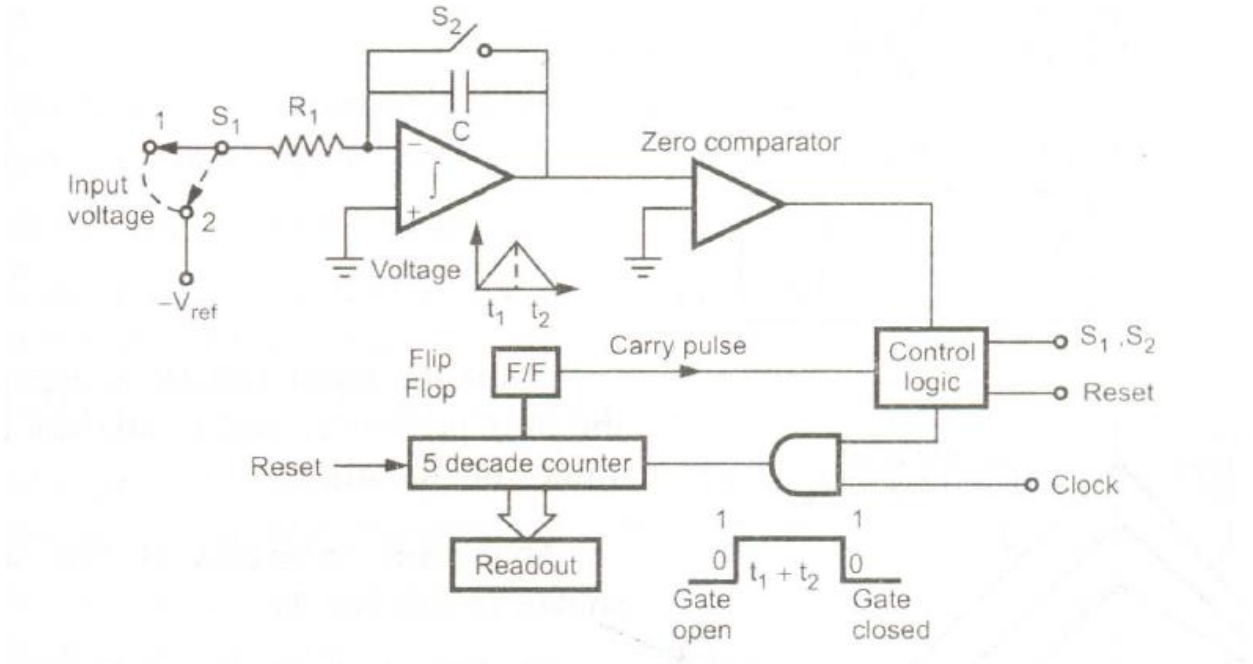
DUAL SLOPE INTEGRATING TYPE DVM

This is the most popular method of analog to digital conversion. In the ramp techniques, the noise can cause large errors but in dual slope method the noise is averaged out by the positive and negative ramps using the process of integration. The basic principle of this method is that the input signal is integrated for a fixed interval of time. And then the same integrator is used to integrate the reference voltage with reverse slope. Hence the name given to the technique is **dual** slope integration technique.

The block diagram of dual slope integrating type DVM is shown in the Fig. It consists of five blocks, an op-amp used as an integrator, a zero comparator, clock pulse generator, a set of decimal counters and a block of control logic.



When the switch Sl is in position 1, the capacitor C starts charging from zero level. The rate of charging is proportional to the input voltage level. The output of the op-amp is given by,

$$V_{out} = -\frac{1}{R_1 C}\int_0^{t_1} V_{in}\, dt$$

$$\therefore \quad \boxed{V_{out} = -\frac{V_{in}\ t_1}{R_1\ C}}$$

where t_1 = Time for which capacitor is charged

V_{in} = Input voltage

R_1 = Series resistance

C = Capacitor in feedback path

After the interval t I, the input voltage is disconnected and a negative voltage -Vref is connected by throwing the switch S1 in position 2. In this position, the output of the op-ilmp is given by,

$$V_{out} = \frac{1}{R_1 C}\int_0^{t_2} -V_{ref}\, dt$$

$$\boxed{V_{out} = -\frac{V_{ref}\ t_2}{R_1\ C}}$$

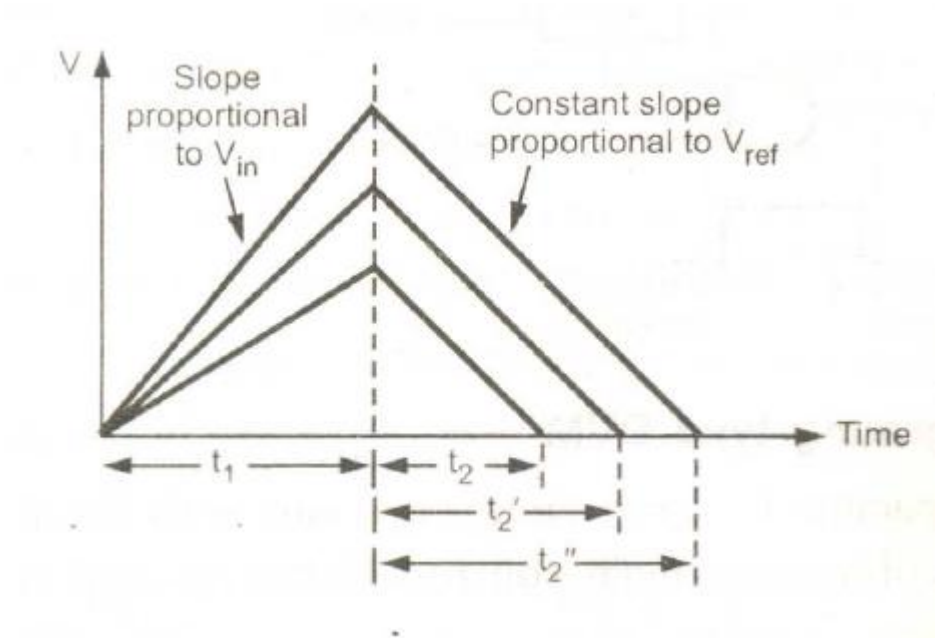
Subtracting (1) from (2),

$$V_{out} - V_{out} = 0 = \frac{-V_{ref}\ t_2}{R_1\ C} - \left(\frac{-V_{in}\ t_1}{R_1\ C}\right)$$

$$\therefore \quad \frac{V_{ref}\ t_2}{R_1\ C} = \frac{V_{in}\ t_1}{R_1\ C}$$

$$\therefore \quad V_{ref}\ t_2 = V_{in}\ t_1$$

$$\therefore \quad \boxed{V_{in} = V_{ref} \cdot \frac{t_2}{t_1}}$$



Thus the input voltage is dependent on the time periods t] and t2 and not on the values of R] and C. This basic principle of this method is shown in the Fig.

At the start of the measurement, the counter is resetted to zero. The output of the flip-flop is also zero. This is given to the control logic. This control sends a signal so as to close an electronic switch to position 1 and integration of the input voltage starts. It continues till the time period t.

As the output of the integrator changes from its zero value, the zero comparator output changes its state. This provides a signal to control logic which inturn opens the gate and the counting of the clock pulses starts.

The counter counts the pulses and when it reaches to 9999, it generates a carry pulse and all digits go to zero. The flip flop output gets activated to the logic level T. This activates the control logic. This sends a signal which changes the switch 5\ position from 1 to 2 Thus -Vref gets connected to op-amp. As Vref polarity is opposite, the capacitor starts discharging. The integrator output will have constant negative slope as shown in th Fig. 3.5"1. The output decreases linearly and after the interval t2, attains zero value, when the capacitor C gets fully discharged.

From equation (3) we can write,

$$V_{in} = V_{ref} \cdot \frac{t_2}{t_1}$$

Let time period of clock oscillator be T and digital counter has counted the counts n1 and n2 during the period t] and t2 respectively.

$$V_{in} = V_{ref} \cdot \frac{n_2 T}{n_1 T} = V_{ref} \cdot \frac{n_2}{n_1}$$

Thus the unknown voltage measurement is not dependent on the clock frequency, but dependent on the counts measured by the counter.

The advantages of this technique are:

i) Excellent noise rejection as noise and superimposed a.c. are averaged out during the process of integration.

ii) The RC time constant does not affect the input voltage measurement.

iii)The capacitor is connected via an electronic switch. This capacitor is an auto zero capacitor and avoids the effects of offset voltage.

iv)The integrator responds to the average value of the input hence sample and hold circuit is not necessary.

v) The accuracy is high and can be readily varied according to the specific requirements.

The only disadvantage of this type of DVM is its slow speed.

Source : http://elearningatria.files.wordpress.com/2013/10/ece-iii-electronic-instrumentation-10it35-notes.pdf