INSTRUCTION SET ARCHITECTURE AND TRENDS

Defining C omputer Arch itecture

The computer designer has to ascertain the attributes that are important for a new computer and design the system to maximize the performance while staying within cost, power and availability constraints. The task has few important aspects such as Instruction Set design, Functional organization, Logic design and implementation.

Instruction Set Architecture (ISA)

ISA refers to the actual programmer visible Instruction set. The ISA serves as boundary between the software and hardware. Th e seven dimensions of the ISA are:

i)Class of ISA: Nearly all ISAs today ar e classified as General-Purpose-Register architectures. The operands are either Registers or Memory locations.
The two popular versions of this class are:
Register-Memory ISAs : ISA of 80x86, can access memory as part of many instructions.
Load -Store ISA Eg. ISA of MIPS, can access memory only with Load or Store instructions.

ii)**Memory addressing**: Byte addressing scheme is most widely used in all desktop and server computers. Both 80x86 and MIPS use byte addressing. Incase of MIPS the object must be aligned. An access to an object of s b yte at byte address A is aligned if A mod s =0. 80x86 does not require alignment. Accesses are faster if operands are aligned.

iii) **Addressing modes**:Specify the address of a M object apart from register and constant operands.
MIPS Addressing modes:
•Register mode addressing
•Immediate mode addressing
•Displacement mode addressing

80x86 in addition to the above addressing modes supports the additional modes of addressing:

i. Register Indirect
ii. Indexed
iii,Based with Scaled index

iv)Types and sizes of operands:

MIPS and x86 support:
•8 bit (ASCII character), 16 bit(Unicode character)
•32 bit (Integer/word)
•64 bit (long integer/ Double word)
•32 bit (IEEE-754 floating point)
•64 bit (Double precision floating point)
•80x86 also supports 80 bit floating point operand.(extended double Precision

v)Operations:The general category o f operations are:

- oData Transfer
- oArithmetic operations
- oLogic operations
- oControl operations
- oMIPS ISA: simple & easy to implement
- ox86 ISA: richer & larger set of operations

vi) Control flow instructions:All ISAs support:
Conditional & Unconditional Branches
Procedure C alls & Returns MIPS 80x86

- Conditional Branches tests content of Register Condition code bits
- Procedure C all JAL CALLF
- Return Address in a R Stack in M

vii) Encoding an ISA

Fixed Length ISA	**Variable Length ISA**
MIPS 32 Bit long	80x86 (1-18 bytes)
Simplifies decoding	Takes less space

Number of Registers and number of Addressing modes hav e significant impact on the length of instruction as the register field and addressing mode field can appear many times in a single instruction.

Trends in Technology

The designer must be aware of the following rapid changes in implementation technology.

- •Integrated C ircuit (IC) Logic technology
- •Memory technology (semiconductor DRAM technology)
- •Storage o r magnetic disk technology
- •Network technology

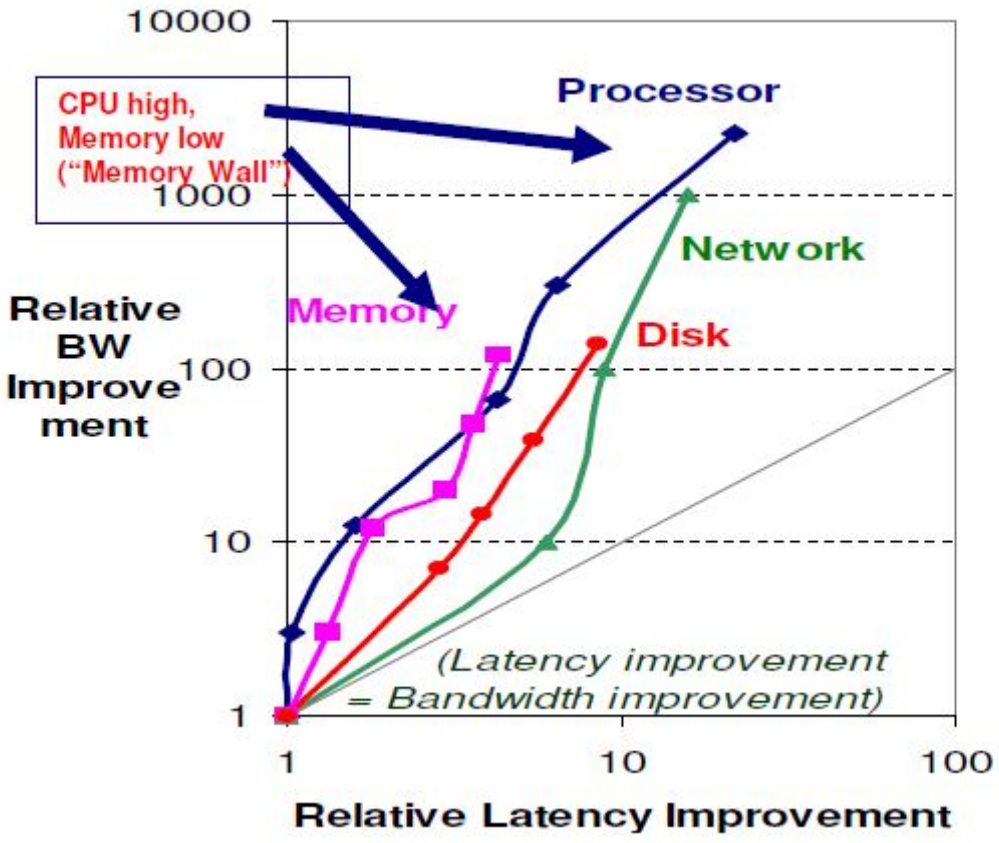
IC Logic technology:

Transistor density increases by about 35%per year. Increase in die size corresponds to about 10 % to 20% per year. The combined effect is a growth rate in transistor count on a chip of about 40% to 55% per year. Semiconductor DRAM technology:cap acity increases by about 40% per year.
Storage Technology:
Before 1990: the storage density increased by about 30% per year.
After 1990: the storage density increased by about 60 % per year.
Disks are still 50 to 100 times cheaper per bit than DRAM.

Network Technology:

Network performance depends both on the per formance of the switches and on the performance of the transmission system. Although the technology improves continuously, the impact of these improvements can be in discrete leaps.

Performance trends: Bandwidth or throughput is the total amount of work done in given time.
Latency or response time is the time between the start and the completion of an event. (for eg. Millisecond for disk access)



A simple rule of thumb is that bandwidth gro ws by at least the square of the improvement in latency. Computer designers should make plans accordingly.

- •IC Processes are characterizes by the f ature sizes.
- •Feature sizes decreased from 10 microns(1971) to 0.09 microns(2006)
- •Feature sizes shrink, devices shrink quadr atically.
- •Shrink in vertical direction makes the operating v oltage of the transistor to reduce.
- •Transistor performance improves linearly with decreasing feature size

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•Transistor count improves quadratically with a linear improvement in Transistor performance.

•!!! Wire delay scales poo rly comp ared to Transistor performance.

•Feature sizes shrink, wires get shorter.

•Signal delay fo r a wire increases in proportion to the product of Resistance and Capacitance.

Trends in Power in Integrated Circuits

For CMOS chips, the dominant source of energy consumption is due to switching transistor, also called as Dynamic power and is given b y the following equation.

Power = (1/2)*Capacitive load* Voltage

* Frequency switched dynamic

•For mobile devices, energy is the better metric

Energy *dynamic* = Capacitive load x Voltage 2

•For a fix ed task, slowing clock rate (frequency switched) reduces power, but not energy

•Capacitive load a function of number of transistors connected to output and technology, which determines capacitance of wires and transistors

•Dropping voltage helps both, so went from 5V down to 1V

•To save energy & dynamic power, most CPUs now turn off clock of inactive modules

•Distributing the power, removing the heat and preventing hot spots have become increasingly difficult challenges.

• The leakage current flows even when a transistor is off. Therefore *static power* is equally important.

$$\text{Power}_{\text{static}} = \text{Current}_{\text{static}} * \text{Voltage}$$

•Leakage current increases in processors with smaller transistor sizes

•Increasing the number of transistors increases power even if they are turned off

•In 2006, goal for leakage is 25% of total power consumption; high performance designs at 40%

•Very low power systems even gate voltage to inactive modules to control loss due to leakage