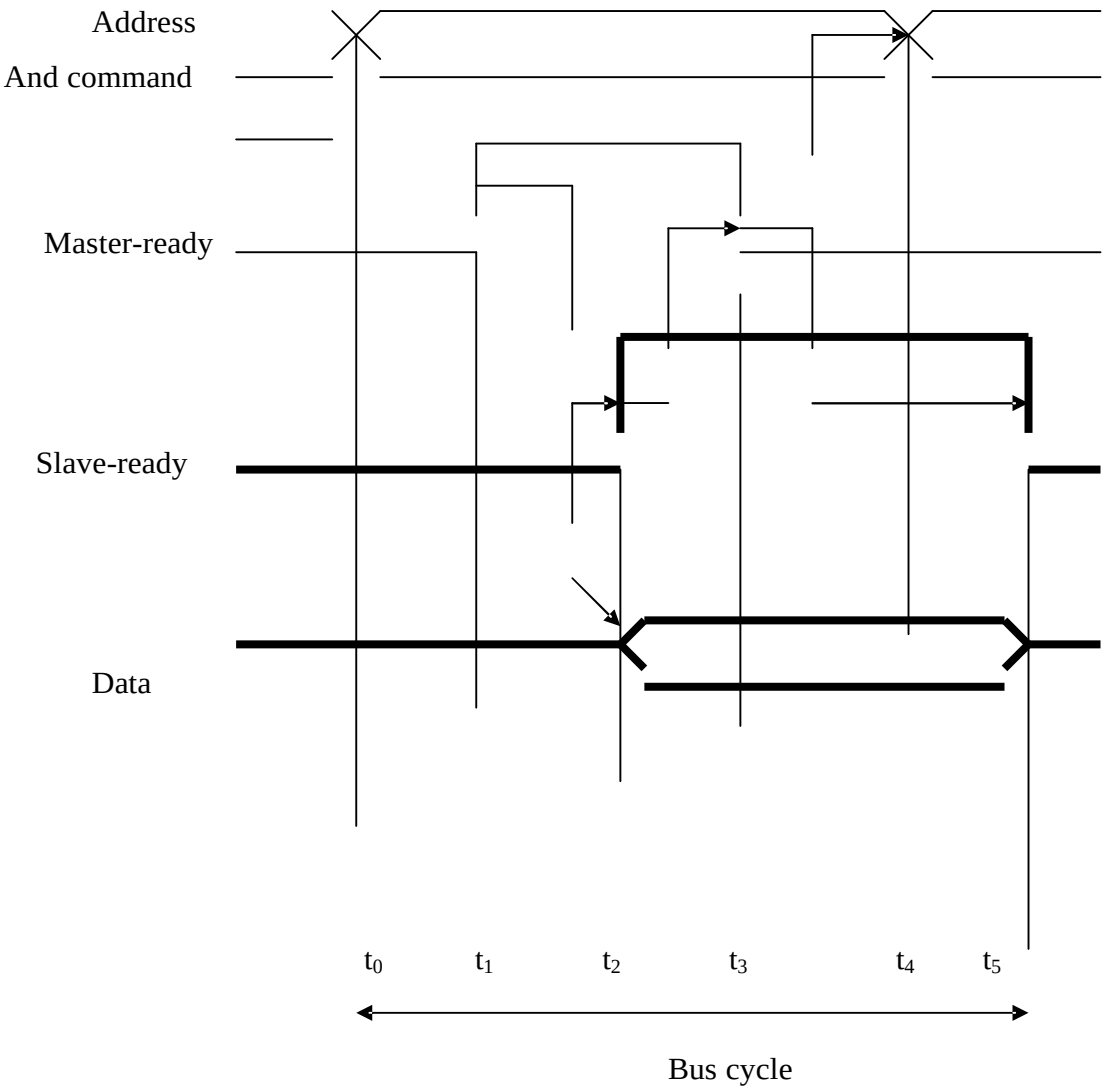
ASYNCHRONOUS BUS

An alternative scheme for controlling data transfers on the bus is based on the use of a handshake between the master and the salve. The concept of a handshake is a generalization of the idea of the Slave-ready signal in figure 10. The common clock is replaced by two timing control lines, Master-ready and Slave-ready. The first is asserted by the master to indicate that it is ready for a transaction, and the second is a response from the slave.

In principle, a data transfer controlled by a handshake protocol proceeds as follows. The master places the address and command information on the bus. Then it indicates to all devices that it has done so by activating the Master-ready line. This causes all devices on the bus to decode the address. The selected slave performs the required operation and informs the processor it has done so by activating the Slave-ready line. The master waits for Slave-ready to become asserted before it removes its signals from the bus. In the case of a read operation, it also strobes the data into its input buffer.

Figure 10 Handshake control of data transfer during an input operation.



An example of the timing of an input data transfer using the handshake scheme is given in figure 4.26, which depicts the following sequence of events.

t_0 – The master places the address and command information on the bus, and all devices on the bus begin to decode this information.

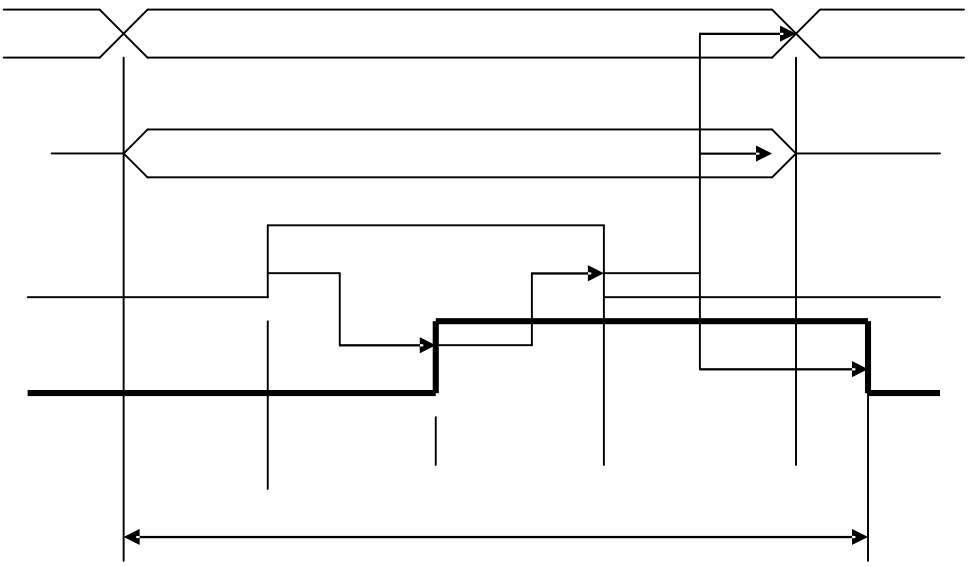
t_1 – The master sets the Master-ready line to 1 to inform the I/O devices that the address and command information is ready. The delay t_1-t_0 is intended to allow for any skew that may occur o the bus. Skew occurs when two signals simultaneously transmitted from one source arrive at the destination at different times. This happens because different lines of the bus may have different propagation speeds. Thus, to guarantee that the Master-ready signal does not arrive at any device ahead of the address and command information, the delay t_1-t_0 should be larger than the maximum possible bus skew.

t_2 – The selected slave, having decoded the address and command information performs the required input operation by placing the data from its data register on the data lines.

t_3 – The Slave-ready signal arrives at the master, indicating that the input data are available on the bus.

t_4 – The master removes the address and command information from the bus. The delay between t_3 and t_4 is again intended to allow for bus skew.

t5 – When the device interface receives the 1 to 0 transition of the Master-ready signal, it removes the data and the Slave-ready signal from the bus. This completes the input transfer.



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