WHAT'S NEXT FOR SEMICONDUCTOR PACKAGING?

With mobile devices continuing to shrink in size and wearable electronics emerging as a new market for semiconductors, advanced packaging technologies are taking on increasing importance in the global supply chain. Aside from the 3DIC package/system-in-package area, what is going on in semiconductor packaging these days?

Flip-chip and wafer-level packaging, among other types of chip-scale packaging (CSP), are progressing in technology development and industry adoption. They are not new technologies, but the multiple types of CSPs continue to proliferate.

Wafer-level chip-scale packaging (WLCSP) is being employed in the iPhone and other mobile devices. TechSearch International forecasts that the number of devices in wafer-level packages will more than double over seven years, reaching nearly 36.8 billion devices in 2017.

STATS ChipPAC, one the world's largest contractors in IC assembly and testing services, recently introduced an encapsulated wafer-level chip-scale package,

which it says can help prevent damage to the chip during the surface-mounting process.

“WLCSP is a bare-die package that is constantly exposed to potential cracking, chipping and handling damages before or during the SMT process. This is particularly true for advanced node products where the die is very thin and dielectric layers are extremely fragile,” Dr. Han Byung Joon, executive vice president and chief technology officer of STATS ChipPAC, said in a statement.

“As mobile device manufacturers tighten their technical specifications to reach new levels of reliability in their products, the industry will see more stringent component level and board-level reliability (BLR) requirements. eWLCSPTM is a robust packaging solution that cost-effectively addresses the increased durability requirements for our customers in advanced silicon nodes down to 28nm.”

Amkor Technology, another large provider of chip assembly and test services, has seen the percentage of its revenue from advanced products (including flip chip, wafer-level processing and related test services) increase from 40.5 percent in 2011 to 49.1 percent in 2013. The company offers three options in WLCSP **— CSPnl bump on repassivation, CSPnl bump on redistribution, and CSPn3. These packages can have from four to 196 solder balls.**

Advanced Semiconductor Engineering**, another of the Big 4 in IC assembly and test services, offers a number of advanced packaging types, such as WLCSP,**

flip-chip CSP, flip-chip package-in-package, flip-chip ball grid array and its Advanced Single Sided Substrate, trademarked as aS 3. These types can accommodate from six to 2,916 leads.

In 2013, ASE saw its percentage of packaging revenue from advanced packaging increase to 26.7 percent from 2012’s 23.6 percent.

There are many other types of advanced packages, including ball grid arrays (BGAs), bump chip carriers (BCCs), and thin quad flat packages (TQFPs). BGAs have a host of variations, such as flip-chip BGAs and thin BGAs. (Packaging is a big bowl of alphabet soup with all its acronyms – that’s another article.) Intel has been using BGA packages since the days of the Pentium II microprocessors and the first Celeron mobile processors. It currently employs a “Micro-FCBGA” package for its mobile processors, containing 479 solder balls.

Land grid arrays, which Intel is making greater use of in the last five years, are basically a BGA without the solder balls.

Bump chip carriers are used in cell phones, digital cameras, wireless local-area networks, and other products.

Amkor touts its thin quad flat packs for application-specific integrated circuits, controllers, digital signal processors, field-programmable gate arrays, PC chipsets, processors, programmable logic devices, and static random-access memories. There are a wide variety of quad flat package types.

Dynamic random-access memories get their own advanced packaging, too. Fine-pitch BGAs are used for high-speed DRAMs.

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