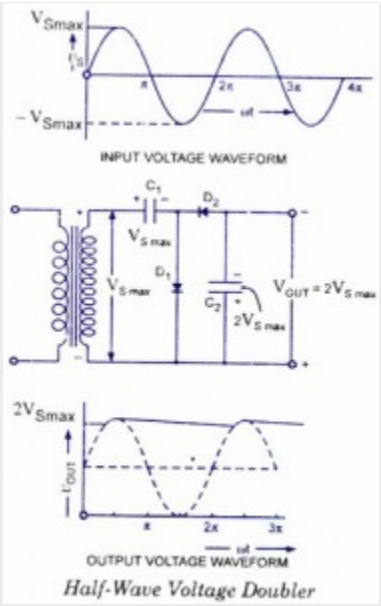
VOLTAGE MULTIPLIERS

Voltage multiplier is a modified capacitor filter circuit that delivers a dc voltage twice or rnore times of the peak value (amplitude) of the input ac voltage. Such power supplies are used for high-voltage and low-current devices such as cathode-ray tubes (the picture tubes in TV receivers, oscilloscopes and computer display). Here we will consider half-wave voltage doubler, full-wave voltage doubler and voltage tripler and quadrupler.

Half-Wave Voltage Doubler

The circuit of a half-wave voltage doubler is given in figure shown below. During the positive half cycle of the ac input, voltage, diode D_1 being forward biased conducts (diode D_2 does not conduct because it is reverse-biased) and charges capacitor C_1 upto peak values of secondary voltage V_{smax} with the polarity, as marked in figure shown below.



Half-wave voltage doubler

During the negative half-cycle of the input voltage diode D_2 gets forward biased and conducts charging capacitor C_2. For the negative half cycle, the lower end of the transformer secondary is positive while upper end is negative. The polarity of the capacitor C_2 has also been marked in the figure. Now starting from the bottom of the transformer secondary and moving clockwise and applying Kirchhoffs voltage law to the outer loop we have

$$\mathbf{-V_{smax} - V_{c1} + V_{c2} = 0}$$

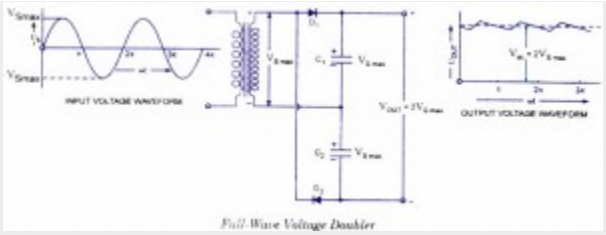
Or

$V_{c2} = V_{smax} + V_{c1} = Vsmax + Vsmax = 2V_{smax}$ = Twice the peak value of the transformer secondary voltage. (Since $V_{c1} = V_{smax}$)

During the next positive half-.cycle diode D_2 is reverse-biased and so acts as an open and capacitor C_2 discharges through the load If there is no load across the capacitor, C_2 both capacitors stay charged – C_1 to V_{smax} and C_2 to $2V_{smax}$. If, as expected there is a load connected to the output terminals of the voltage doubler, the capacitor C_2discharges a little bit and consequently the voltage across capacitor C_2 drops slightly. The capacitor C_2 gets recharged again in the next half-cycle. The ripple frequency in this case will be the signal frequency (that is, 50 Hz for supply mains.)

Full-Wave Voltage Doubler

The circuit diagram for a full-wave voltage doubler is given in the figure shown below. During the positive cycle of the ac input voltage, diode D_1 gets forward biased and so conducts charging the capacitor C_1 to a peak voltage V_{smax} with polarity indicated in the figure, while diode D_2 is reverse-biased and does not conduct.During the negative half-cycle, diode D_2 being forward biased conducts and charges the capacitor C_2 with polarity shown in the figure while diode D_1 does not conduct. With no load connected to the output terminals, the output voltage will be equal to sum of voltages across capacitors C_1 and C_2 that is, $V_{C1} + V_{C2}$ or $(V_{s\ max} + V_{s\ max})$ or $2\ V_{s\ max}$. When the load is connected to the output terminals, the output voltage V_L will be somewhat less than $2\ V_{s\ max}$. The input voltage and output voltage waveforms are also shown in the figure below.



Full-wave voltage doubler

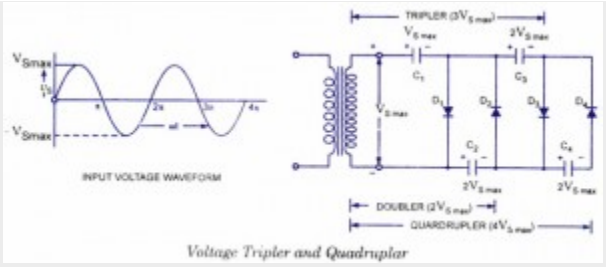
Take a look : Comparison Between Half-wave and Full-wave Voltage Doublers

Voltage Tripler and Quadruples

The half-wave voltage doubler, shown in the earlier figure can be extended to provide any multiple of the peak input voltage (that is, $3\ V_{s\ max}$, $4\ V_{s\ max}$ or $5\ V_{s\ max}$), as illustrated in the figure shown below. It is obvious from the pattern of the circuit connections how additional diodes and capacitors are to be connected to provide output voltage, 5,6,7 or 8 times the peak input voltage from a supply transformer of rating only $V_{s\ max}$, and each diode in the circuit of PIV rating $2\ V_{s\ max}$. If load is small and the capacitors have little leakage, extremely high dc voltages can be obtained from such a circuit using many sections to step-up the dc voltage.

In operation capacitor C_1 is charged through diode D_l to a peak value of transformer secondary voltage, $V_{s\ max}$during first positive half-cycle of the ac input voltage. During the negative half cycle capacitor C_2 is charged to twice the peak voltage 2 V_s developed by the sum of voltages across capacitor C_1 and the transformer secondary. During the second positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges the capacitor C_3 to the same 2 $V_{g\ max}$ peak voltage. During the negative half-cycle diodes D_2 and D_4 conduct allowing capacitor C_3 to charge capacitor C_4 to peak voltage 2 $V_{S\ max}$. From the fogure shown below it is obvious that the voltage across capacitor C_2 is 2 $V_{s\ max}$, across capacitors C_1 and C_3 it is 3 $V_{s\ max}$ and across capacitors C_2 and C_4 it is 4 V_{smax}.

If additional diodes (each diode of PIV rating 2 $V_{s\ max}$) and capacitors (each capacitor of voltage rating 2 $V_{s\ max}$) are used, each capacitor will be charged to 2 $V_{s\ max}$. Measuring from the top of the transformer secondary winding (figure below) will give odd multiples of $V_{g\ max}$ at the output, while measuring from the bottom of transformer secondary winding will give even multiples of the peak voltage, $V_{s\ max}$.



Voltage Tripler and Quadruplar

Some electronic devices, such as cathode ray tubes (in picture tubes in TV receivers, oscilloscopes and computer display) need dc power supply at high voltage with low current. This requirement can be met with either by employing a step-up transformer with a rectifier circuit or by employing voltage multiplier. Since transformers are very bulky and costly, voltage multipliers are preferred. By using voltage multipliers, the voltage level is usually raised well into the hundreds or thousands of volts.

Generally such circuits are employed when both the supply voltage and load are maintained constant

Source : http://www.circuitstoday.com/voltage-multipliers