VERTICAL INTERCONNECT TECHNOLOGIES (3-D ICS)

3-D IC design strategies are also known as vertical interconnect technologies as they basically exploit the vertical dimension of the chip to reduce interconnect length and to achieve greater integration efficiency.

The techniques are:

- **Wire-bonding**
- **Micro-bumps**
- **Through-vias**
- **Contact less interconnect**

Each 3-D technology has its own pros and cons. However, all of them provide better handling of interconnect delays in very deep sub micron devices. Comparisons of the method of assembly (die-scale or wafer-scale), maximum number of tiers, vertical interconnects pitch and the amount of routing resources consumed on the chip is shown in Table (1). Figure (1) shows a summary of different 3D interconnect approaches.

		Assembly	Tier limit	Vertical Pitch	Chip Layer Resources
Wire-bonded		Die	~5	35-100μm	All
Micro-bump	3D Package	Die	heat	25-50μm	Top 1-2
	Face-to-face	Die	2	10-100μm	Top 1-2
Contactless	Capacitive	Die	2	50-200μm	Top
	Inductive	Die	heat	50-150μm	Top 1-2
Through-Via	Bulk	Wafer	heat, yield	50μm	All + Top
	SOI	Wafer	heat, yield	5μm	All + Top

Table (1) Comparison of Vertical Interconnect Technologies [5]

Wire-bonded

Individual die are stacked and wire-bonded in this technique. Connections between chips are made through the board or chip-carrier and back to other chips in the stack. This approach is limited by the resolution of wire-bonders (35μm and 15μm) and larger number of I/Os in the IC stack limit the wire-bond technique. To protect the pad from tearing off due to mechanical stresses during bond process, all metal layers are required.

Micro-bump technology

In this technology connections are made using solder or gold bumps on the surface of die. Typically the pitch of the bumps is 50-500µm. Epoxy routing tier has micro bump bonded to it and this brings the signals to the edges of the cube, these different tiers are then stacked together. Since assembly related mechanical stresses are less the pads require maximum two layers. Here dies are assembled into a cube. Compared to wire bond technology micro bump technology provide greater vertical interconnect density. Since signals have to be routed to the periphery of the chip no significant reduction of parasitic capacitance can be achieved. Heat generated inside the cube limits the number of tiers that can be stacked. As observed by the authors in [5] with proper placement of blocks in the 3D architecture, the use of high-power dynamic logic circuits, repeaters, pipelined stages long routing paths could be reduced and this decreases overall power consumption by 15% while simultaneously increasing performance by 15%.

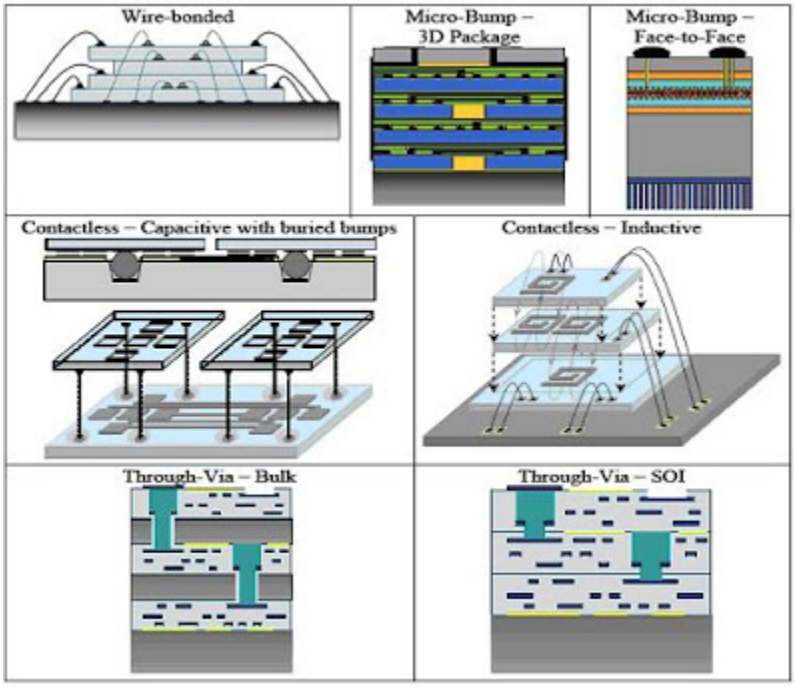

Figure (1) Different 3-D IC technologies [5]

Through-Via interconnect

There are two types of through via interconnect technologies available. They are: through via bulk and through via Silicon on Insulator (SOI). Both methods have the potential to offer the greatest interconnect density with disadvantage of the greatest cost. The first and second wafers are placed face to face and as the tier grows higher layers are placed face to back. Connection is provided by filling tungsten in etched wafers. The next chip sits on the

polished surface of the previously etched chip. Power, ground, and I/O connectivity is provided by the top tier. Number of tiers is mainly limited by the heat generated inside the stack. Lesser the tier number higher is the yield. Through via Silicon on Insulator technology has achieved smallest inter tier pitch of the order of 5µm. all layers in the upper tiers and the top layer in the lower tier is consumed in this technology.

Contact less interconnect technology

Contact less or AC-coupled interconnect use capacitive or inductive coupling to communicate between tiers. This method eliminates the signal interconnect connection to the periphery of the IC as well as inter-tier routing. Half capacitors formed by top level of metal are used on capacitive coupling. The distance between the tiers, the rise/fall times of the technology, and the dielectric constant of the gap decide the density of these interconnects. Half capacitors approach requires the tiers to be face-to-face. This limits the number of tiers to two. Power supply between chips is provided by the help of bumps. The distance between two half plates should be small. Either high-k dielectric or trench formation is used to achieve better capacitive coupling. Inductive coupling is more suitable wherein separation of the coupling elements is of the order of lateral dimension of the coupling elements.

Source : http://asic-soc.blogspot.in/2007/11/vertical-interconnect-technologies-3-d.html