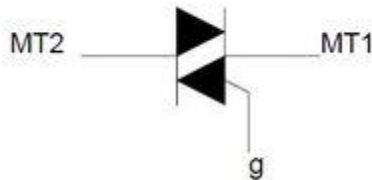


# Triac - Basic Concepts

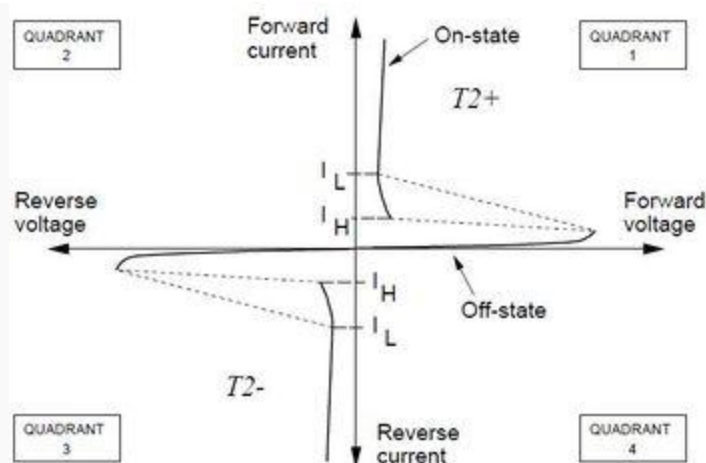
## Introduction



Triac

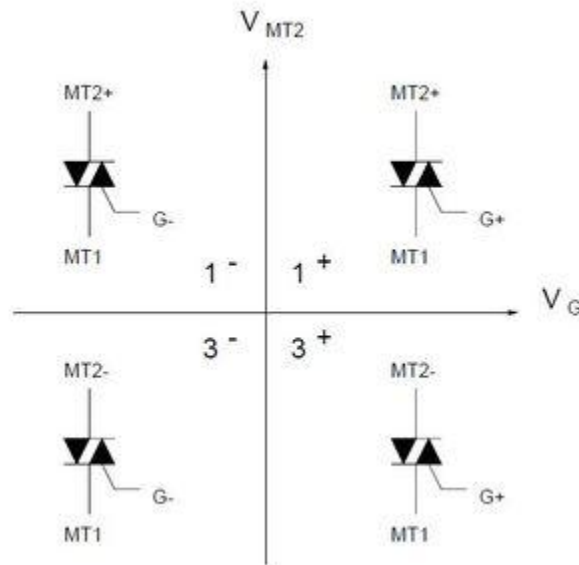
A triac can be regarded as a "bidirectional thyristor" because it conducts in both directions. For standard triacs, current flow in either direction between the main terminals MT1 and MT2 is initiated by a small signal current applied between MT1 and the gate terminal.

## Turn-On



Triac U-I characteristic

Unlike [thyristors](#), standard triacs can be triggered by positive or negative current flow between the gate and MT1. (The rules for  $V_{GT}$ ,  $I_{GT}$  and  $I_L$  are the same as for [thyristors](#). See [Rule 1](#).) This permits triggering in four "quadrants".



Triac triggering quadrants

Where the gate is to be triggered by DC or unipolar pulses at zero-crossing of the load current, negative gate current is to be preferred for the following reasons. The internal construction of the triac means that the gate is more remote from the main current-carrying region when operating in the 3+ quadrant. This results in:

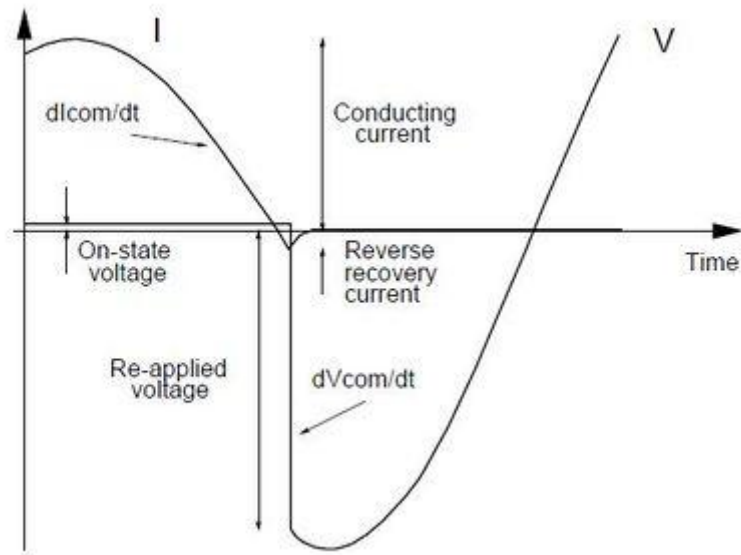
- 1. Higher  $I_{GT}$  -> higher peak  $I_G$  required,
- 2. Longer delay between  $I_G$  and the commencement of load current flow -> longer duration of  $I_G$  required,
- 3. Much lower  $dI_T/dt$  capability -> progressive gate degradation can occur when controlling loads with high initial  $dI/dt$  (e.g. cold incandescent lamp filaments),
- 4. Higher  $I_L$  (also true for 1- operation) -> longer  $I_G$  duration might be needed for very small loads when conducting from the beginning of a mains half cycle to allow the load current to reach the higher  $I_L$ .

In standard AC phase control circuits such as lamp dimmers and domestic motor speed controls, the gate and MT2 polarities are always the same. This means that operation is always in the 1+ and 3- quadrants where the triac's switching parameters are the same. This results in symmetrical triac switching where the gate is at its most sensitive.

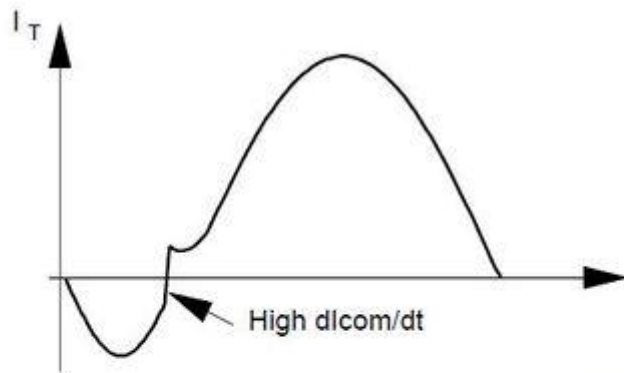
Note:- The 1+, 1-, 3- and 3+ notation for the four triggering quadrants is used for brevity instead of writing "MT2+, G+" for 1+, etc. It is derived from the graph of the triac's U-I characteristic. Positive MT2 corresponds with positive current flow into MT2, and vice versa. Hence, operation is in quadrants 1 and 3 only. The + and - superscripts refer to inward and outward gate current respectively.

**Rule 3.** When designing a triac triggering circuit, avoid triggering in the 3+ quadrant (MT2-, G+) where possible.

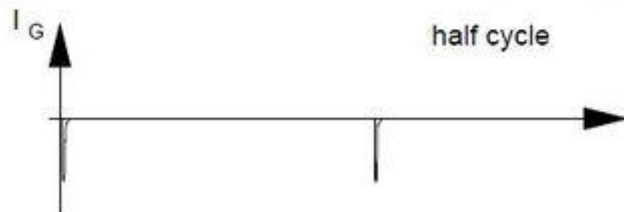
## Alternative turn-on methods



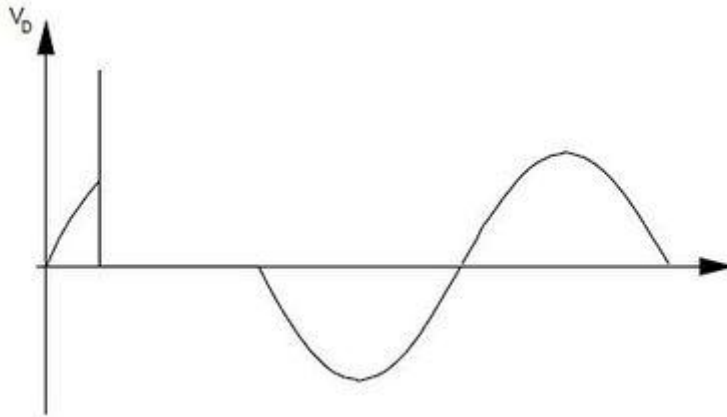
Triac  $dI_{COM}/dt$  and  $dV_{COM}/dt$  (b)



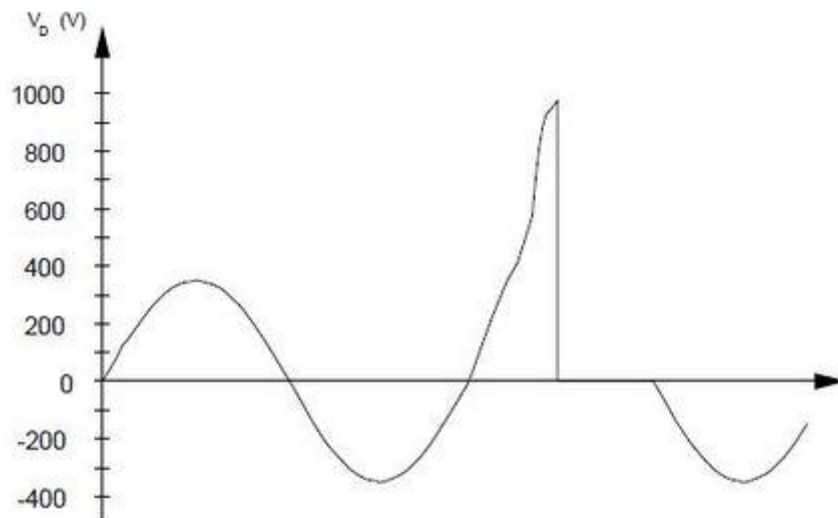
Commutation failure causes  
conduction at beginning of  
half cycle



Effects of rectifier-fed inductive load on phase control circuit (c)



Triac turn-on by exceeding  $dV_D/dt$  (d)



Triac turn-on by exceeding  $dV_{DRM}/dt$  (e)

There are undesirable ways a triac can be turned on. Some are benign, while some are potentially destructive.

- **(a) Noisy gate signal**

In electrically noisy environments, spurious triggering can occur if the noise voltage on the gate exceeds  $V_{GT}$  and enough gate current flows to initiate regenerative action within the triac. The first line of defence is to minimise the occurrence of the noise in the first place. This is best achieved by keeping the gate connections as short as possible and ensuring that the common return from the gate drive circuit connects directly to the MT1 pin (or cathode in the case of a thyristor). In situations where the gate connections are hard wired, twisted pair wires or even shielded cable might be necessary to minimise pickup. Additional noise immunity can be provided by adding a resistor of  $1k\Omega$

or less between the gate and MT1 to reduce the gate sensitivity. If a high frequency bypass capacitor is also used, it is advisable to include a series resistor between it and the gate to minimise peak capacitor currents through the gate and minimise the possibility of overcurrent damage to the triac's gate area. Alternatively, use a series H triac (e.g. BT139-600H). These are insensitive types with 10mA min IGT specs which are specifically designed to provide a high degree of noise immunity.

**Rule 4.** To minimise noise pickup, keep gate connection length to a minimum. Take the return directly to MT1 (or cathode). If hard wired, use twisted pair or shielded cable. Fit a resistor of 1k $\Omega$  or less between gate and MT1. Fit a bypass capacitor in conjunction with a series resistor to the gate. Alternatively, use an insensitive series H triac.

▪ **(b) Exceeding the max rate of change of commutating voltage  $dV_{COM}/dt$**

This is most likely to occur when driving a highly reactive load where there is substantial phase shift between the load voltage and current waveforms. When the triac commutates as the load current passes through zero, the voltage will not be zero because of the phase shift. The triac is then suddenly required to block this voltage. The resulting rate of change of commutating voltage can force the triac back into conduction if it exceeds the permitted  $dV_{COM}/dt$ . This is because the mobile charge carriers have not been given time to clear the junction. The  $dV_{COM}/dt$  capability is affected by two conditions:

1. The rate of fall of load current at commutation,  $dI_{COM}/dt$ . Higher  $dI_{COM}/dt$  lowers the  $dV_{COM}/dt$  capability.
2. The junction temperature  $T_j$ . Higher  $T_j$  lowers the  $dV_{COM}/dt$  capability.

If the triac's  $dV_{COM}/dt$  is likely to be exceeded, false triggering can be avoided by use of an RC snubber across MT1-MT2 to limit the rate of change of voltage. Common values are 100 $\Omega$  carbon composition resistor, chosen for its surge current handling, and 100nF. **Alternatively, use a Hi-Com triac.** Note that the resistor should never be omitted from the snubber because there would then be nothing to prevent the capacitor from dumping its charge into the triac and creating damaging  $dI_T/dt$  during unfavourable turn-on conditions.

▪ **(c) Exceeding the max rate of change of commutating current  $dI_{COM}/dt$**

Higher  $dI_{COM}/dt$  is caused by higher load current, higher mains frequency (assuming sinewave current) or non sinewave load current. A well known cause of non sinewave load current and high  $dI_{COM}/dt$  is rectifier-fed inductive loads. These can often result in commutation failure in standard triacs as the supply voltage falls below the back EMF of the load and the triac current collapses suddenly to zero. During this condition of zero triac current, the load current will be "freewheeling" around the bridge rectifier circuit. Loads of this nature can generate such high  $dI_{COM}/dt$  that the triac cannot support even the gentle reapplied  $dV/dt$  of a 50Hz waveform rising from zero volts. There will then be no benefit in adding a snubber across the triac because  $dV_{COM}/dt$  is not the problem. The  $dI_{COM}/dt$  will have to be limited by adding an inductor of a few mH in series with the load. **Alternatively, use a Hi-Com triac.**

▪ **(d) Exceeding the max rate of change of off-state voltage  $dV_D/dt$**

If a very high rate of change of voltage is applied across a non-conducting triac (or sensitive gate thyristor in particular) without exceeding its  $V_{DRM}$ , internal capacitive current can generate enough gate current to trigger the device into conduction. Susceptibility is increased at high temperature. Where this is a problem, the  $dV_D/dt$  must be limited by an RC snubber across MT1 and MT2 (or anode and cathode). **In the case of triacs, using Hi-Com types can yield benefits.**

**Rule 5.** Where high  $dV_D/dt$  or  $dV_{COM}/dt$  are likely to cause a problem, fit an RC snubber across MT1 and MT2. Where high  $dI_{COM}/dt$  is likely to cause a problem, fit an inductor of a few mH in series with the load. **Alternatively, use a Hi-Com triac.**

▪ **(e) Exceeding the repetitive peak off-state voltage  $V_{DRM}$**

If the MT2 voltage exceeds  $V_{DRM}$  such as might occur during severe and abnormal mains transient conditions, MT2-MT1 leakage will reach a point where the triac will spontaneously break over into conduction. If the load permits high inrush currents to flow, extremely high localised current density can occur in the small area of silicon that is conducting. This can lead to burnout and destruction of the die. Incandescent lamps, capacitive loads and crowbar protection circuits are likely causes of high inrush currents. Turn-on by exceeding the triac's  $V_{DRM}$  or  $dV_D/dt$  is not necessarily the main threat to its survival. It's the  $dI_T/dt$  that follows which is most likely to cause the damage. Due to the time required for conduction to spread out over the whole junction, the permitted  $dI_T/dt$  is lower than if the triac is correctly turned on by a gate signal. If the  $dI_T/dt$  can be limited during these conditions to this lower value, which is given in data, the triac is more likely to survive. This could be achieved by fitting a non saturable (air cored) inductor of a few  $\mu H$  in series with the load. If the above solution is unacceptable or impractical, an alternative solution would be to provide additional filtering and clamping to prevent the spikes reaching the triac. This would probably involve the use of a Metal Oxide Varistor as a "soft" voltage clamp across the supply, with series inductance followed by parallel capacitance upstream of the MOV.

Doubts have been expressed by some manufacturers over the reliability of circuits which use MOVs across the mains, since they have been known to go into thermal runaway in high ambient temperatures and fail catastrophically. This is due to the fact that their operating voltage possesses a marked negative temperature coefficient. However, if the recommended voltage grade of 275V RMS is used for 230V mains, the risk of MOV failure should be negligible. Such failures are more likely if 250V RMS MOVs are used, which are underspecified for 230V RMS use at high ambient temperatures.

**Rule 6.** If the triac's  $V_{DRM}$  is likely to be exceeded during severe mains transients, employ one of the following measures:

1. Limit high  $dI_T/dt$  with a non saturable inductor of a few  $\mu H$  in series with the load;
2. Use a MOV across the mains in combination with filtering on the supply side.

**Turn-on  $dI_T/dt$**

When a triac or thyristor is triggered into conduction by the correct method via its gate, conduction begins in the die area immediately adjacent to the gate, then quickly spreads to cover the whole active area. This time delay imposes a limit on the permissible rate of rise of load current. A  $dI_T/dt$  which is too high can cause localised burnout. An MT1-MT2 short will be the result. If triggering in the 3+ quadrant, an additional mechanism further reduces the permitted  $dI_T/dt$ . It is possible to momentarily take the gate into reverse avalanche breakdown during the initial rapid current rise. This might not lead to immediate failure. Instead, there would be progressive burnout of the gate-MT1 shorting resistance after repeated exposure. This would show itself by a progressive increase in  $I_{GT}$  until the triac will no longer trigger. Sensitive triacs are likely to be the most susceptible. Hi-Com triacs are not affected as they do not operate in the 3+ quadrant. The  $dI_T/dt$  capability is affected by how fast the gate current rises ( $dI_G/dt$ ) and the peak value of  $I_G$ . Higher values of  $dI_G/dt$  and peak  $I_G$  (without exceeding the gate power ratings) give a higher  $dI_T/dt$  capability.

**Rule 7.** Healthy gate drive and avoiding 3+ operation maximises the triac's  $dI_T/dt$  capability.

As mentioned previously, a common load with a high initial surge current is the incandescent lamp which has a low cold resistance. For resistive loads such as this, the  $dI_T/dt$  would be at its highest if conduction commenced at a peak of the mains voltage. If this is likely to exceed the triac's  $dI_T/dt$  rating, it should be limited by the inclusion of an inductor of a few  $\mu\text{H}$  or even a Negative Temperature Coefficient thermistor in series with the load. Again, the inductor must not saturate during the maximum current peak. If it does, its inductance would collapse and it would no longer limit the  $dI_T/dt$ . An air cored inductor meets the requirement. A more elegant solution which could avoid the requirement for a series current-limiting device would be to use zero voltage turn-on. This would allow the current to build up more gradually from the beginning of the sinewave. Note: It is important to remember that zero voltage turn-on is only applicable to resistive loads. Using the same method for reactive loads where there is phase shift between voltage and current can cause "halfwaving" or unipolar conduction, leading to possible saturation of inductive loads, damagingly high peak currents and overheating. More advanced control employing zero current switching and / or variable trigger angle is required in this case.

**Rule 8.** If the triac's  $dI_T/dt$  is likely to be exceeded, an air cored inductor of a few  $\mu\text{H}$  or an NTC thermistor should be fitted in series with the load. Alternatively, employ zero voltage turn-on for resistive loads.

## Turn-off

Since triacs are used in AC circuits, they naturally commutate at the end of each half cycle of load current unless a gate signal is applied to maintain conduction from the beginning of the next half cycle. The rules for IH are the same as for the thyristor. See [Rule 2](#).

## Hi-Com triac

Hi-Com triacs have a different internal construction to conventional triacs. One of the differences is that the two "thyristor halves" are better separated to reduce the influence that they have on each other. This has yielded two benefits:

1. Higher  $dV_{COM}/dt$ . This enables them to control reactive loads without the need for a snubber in most cases while still avoiding commutation failure. This reduces the component count, board size and cost, and eliminates snubber power dissipation.
2. Higher  $dI_{COM}/dt$ . This drastically improves the chances of successfully commutating higher frequency or non sinewave currents without the need for a  $dI_{COM}/dt$ -limiting inductor in series with the load.
3. Higher  $dV_D/dt$ . Triacs become more sensitive at high operating temperatures. The higher  $dV_D/dt$  of Hi-Com triacs reduces their tendency to spurious  $dV/dt$  turn-on when in the blocking state at high temperature. This enables them to be used in high temperature applications controlling resistive loads, such as cooking or heating applications, where conventional triacs could not be used.

The different internal construction also means that 3+ triggering is not possible. This should not be a problem in the vast majority of cases because this is the least

desirable and least used triggering quadrant, so direct substitution of a Hi-Com for an equivalent conventional triac will almost always be possible.

## Triac mounting methods

For small loads or very short duration load current (i.e. less than 1 second), it might be possible to operate the triac in free air. In most cases, however, it would be fixed to a heatsink or heat dissipating bracket. The three main methods of clamping the triac to a heatsink are clip mounting, screw mounting and riveting. Mounting kits are available from many sources for the first two methods. Riveting is not a recommended method in most cases.

**Rule 9.** Avoid mechanical stress to the triac when fitting it to the heatsink. Fix, then solder. Never pop rivet with the rivet mandrel on the tab side.

## Thermal resistance

Thermal resistance  $R_{th}$  is the resistance to the flow of heat away from the junction. It is analogous to electrical resistance; i.e. just as electrical resistance  $R = V/I$ , thermal resistance  $R_{th} = T/P$ , where  $T$  is the temperature rise in Kelvin and  $P$  is the power dissipation in Watts. Therefore  $R_{th}$  is expressed in K/W. For a device mounted vertically in free air, the thermal resistance is dictated by the junction-to-ambient thermal resistance  $R_{th j-a}$ . This is typically 100K/W for the SOT82 package, 60K/W for the SOT78 package and 55K/W for the isolated F-pack and X-pack. For a non isolated device mounted to a heatsink, the junction-to-ambient thermal resistance is the sum of the junction-to-mounting base, mounting base-to-heatsink and heatsink-to-ambient thermal resistances.

$$R_{th j-a} = R_{th j-mb} + R_{th mb-h} + R_{th h-a} \text{ (non isolated package).}$$

The use of heat transfer compound or sheet between the device and heatsink is always recommended. In the case of isolated packages, there is no reference made to "mounting base", since the  $R_{th mb-h}$  is assumed to be constant and optimised with heat transfer compound. Therefore, the junction-to-ambient thermal resistance is the sum of the junction-to-heatsink and heatsink-to-ambient thermal resistances.

$$R_{th j-a} = R_{th j-h} + R_{th h-a} \text{ (isolated package).}$$

$R_{th j-mb}$  or  $R_{th j-h}$  are fixed and can be found in data for each device.

$R_{th mb-h}$  is also given in the mounting instructions for several options of insulated and non-insulated mounting, with or without heatsink compound.

$R_{th h-a}$  is governed by the heatsink size and the degree of unrestricted air movement past it.

**Rule 10.** For longterm reliability, ensure that the  $R_{th j-a}$  is low enough to keep the junction temperature within  $T_j \text{ max}$  for the highest expected ambient temperature.

Source:

<http://www.openelectrical.org/wiki/index.php?title=Triac>