

# TRANSMISSION GATE

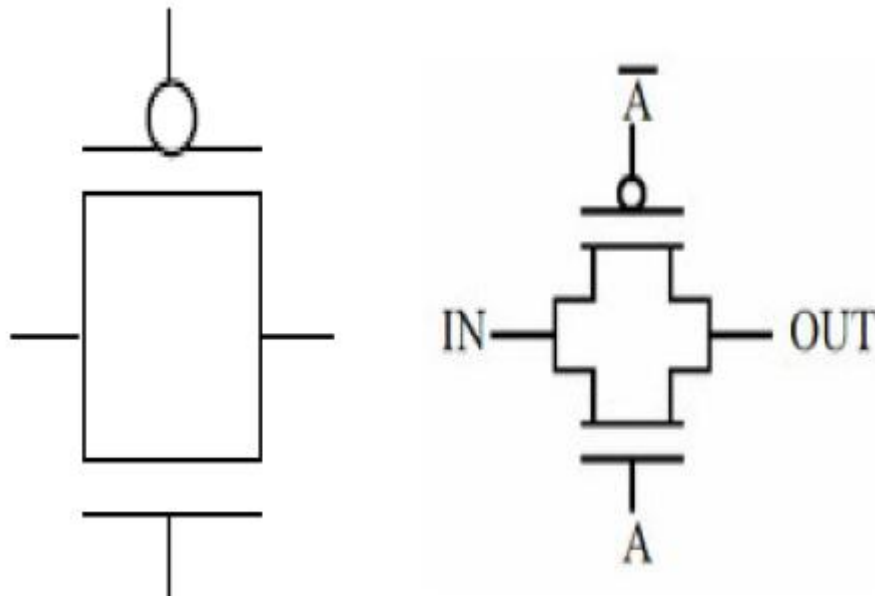


Figure 27: Symbol and schematic of transmission gate

Layout considerations of transmission gate. It consists of drains and the sources of the P&N devices paralleled. Transmission gate can replace the pass transistors and has the advantage of giving both a good one and a good zero.

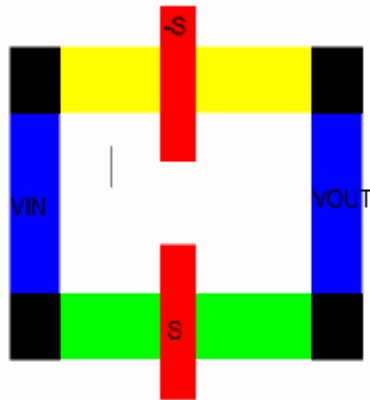


Figure 28: layout of transmission gate.

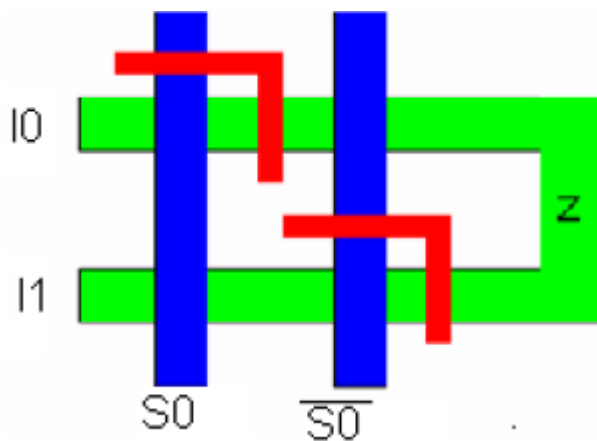


Figure 29: TG with nmos switches.

## 2.8 CMOS STANDARD CELL DESIGN

Geometric regularity is very important to maintain some common electrical characteristics between the cells in the library. The common physical limitation is to fix the height and vary the width according to the required function. The  $W_p$  and  $W_n$  are fixed considering power dissipation, propagation delay, area and noise immunity. The best thing to do is to fix a required objective function and then fix  $W_n$  and  $W_p$  to obtain the required objective. Usually in CMOS  $W_n$  is made equal to  $W_p$ . In the process of designing these gates techniques may be employed to automatically generate the gates of common size. Later optimization can be carried out to achieve a specific feature. Gate array layout and sea of gate layout are constructed using the above techniques.

The gate arrays may be customized by having routing channels in between array of gates. The gate array and the sea of gates have some special layout considerations. **The gate arrays** use fixed image of the under layers i.e. the diffusion and poly are fixed and metal are programmable.

The wiring layers are discretionary and providing the personalization of the array. The rows of transistors are fixed and the routing channels are provided in between them. Hence the design issue involves size of transistors, connectivity of poly and the number of routing channels required. Sea of gates in this style continuous rows of n and p diffusion run across the master chip and are arranged without regard to the routing channel. Finally the routing is done across unused transistors saving space.

Source : <http://elearningatria.files.wordpress.com/2013/10/ece-v-fundamentals-of-cmos-vlsi-10ec56-notes.pdf>