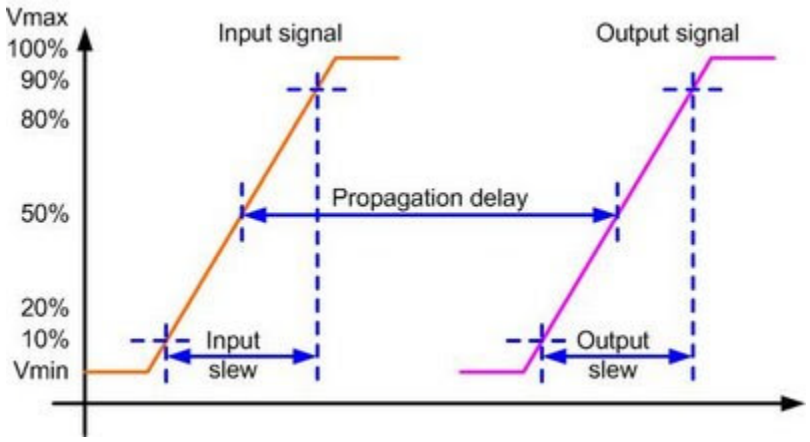
TRANSITION DELAY AND PROPAGATION DELAY

Transition Delay

Transition delay or slew is defined as the time taken by signal to rise from 10 %(20%) to the 90 %(80%) of its maximum value. This is known as “rise time”.



Similarly “fall time” can be defined as the time taken by a signal to fall from 90 %(80%) to the 10 %(20%) of its maximum value.

Transition is the time it takes for the pin to change state.

Setting Transition Time Constraints

The above theoretical definitions are to be applied on practical designs. Now, the transition time of a net becomes the time required for its driving pin to change logic values (from 10 %(20%) to the 90 %(80%) of its maximum value). This transition time used foe delay calculations are based on the timing library (.lib files).

Transition related constraints can be provided in Design Compiler (logic synthesis tool from Synopsys) by using below commands:

1. ***max_transition*** : This attribute is applied to each output of a cell. During optimization, Design Compiler tries to make the transition time of each net less than the value of the***max_transition*** attribute.

2. ***set_max_transition***: This command is used to change the maximum transition time restriction specified in a technology library.

“This command sets a maximum transition time for the nets attached to the identified ports or to all the nets in a design by setting the ***max_transition*** attribute on the named objects.

For example, to set a maximum transition time of 3.2 on all nets in the design adder, enter the following command:

set_max_transition 3.2 [get_designs adder]

To undo a ***set_max_transition*** command, use the ***remove_attribute*** command. For example, enter the following command:

remove_attribute [get_designs adder] max_transition”

(Directly quoted from Design Complier user manual)

Setting Capacitance Constraints

The transition time constraints specified above do not provide a direct way to control the actual capacitance of nets. To control capacitance directly, below command has to be used:

set_max_capacitance: This command sets the maximum capacitance constraint on input ports or designs.

In addition to ***set_max_transition***, ***set_max_capacitance*** can also be used as this command works independent.

This command applies maximum capacitance limit to output pin or port of the design.

This command can also be used to apply capacitance limit on any net.

Eg:

set_max_capacitance 4 [get_designs decoder]

To remove the ***set_max_capacitance*** command, use the ***remove_attribute*** command.

remove_attribute [get_designs decoder] max_capacitance

Propagation Delay

Propagation delay is the time required for a signal to propagate through a gate or net.

Hence if it is cell, you can call it as “Gate or Cell Delay” or if it is net you can call it as “Net Delay”

Propagation delay of a gate or cell is the time it takes for a signal at the input pin to affect the output signal at output pin.

For any gate propagation delay is measured between 50% of input transition to the corresponding 50% of output transition.

There are 4 possibilities:

Propagation delay between 50 % of Input rising to 50 % of output rising.

Propagation delay between 50 % of Input rising to 50 % of output falling.

Propagation delay between 50 % of Input falling to 50 % of output rising.

Propagation delay between 50 % of Input falling to 50 % of output falling.

Each of these delays has different values. Maximum and minimum values of these set are very important. Maximum and minimum propagation delay values are considered for timing analysis.

For net propagation delay is the delay between the time a signal is first applied to the net and the time it reaches other devices connected to that net.

Propagation delay is taken as the average of rise time and fall time i.e. Tpd= (Tphl+Tplh)/2.

Propagation delay depends on the input transition time (slew rate) and the output load. Hence two dimensional look up tables are used to calculate these delays. How to calculate propagation delay of net and gate? Please refer below articles to find the detailed explanation.

Source : http://asic-soc.blogspot.in/2008/12/transition-delay-and-propagation-delay.html