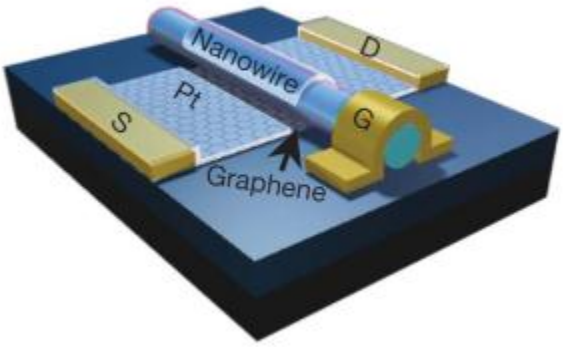
THE THING WITH GRAPHENE TRANSISTORS

Graphene is one of the hottest research areas in nanotechnology, and it may seem slightly surprising it took me a month to write my first blog post on the topic. That moment has now come, with the advance publication of a *Nature* paper that presents highly attractive graphene transistor, even though in my humble opinion the approach taken seems not the most promising for future highly integrated devices.

There are many reasons why graphene gets researchers so excited. The stability of this single layer of carbon atoms is one of the reasons, promising tough composite materials with increased mechanical strength. The unusual electronic properties that in some respect resemble that of relativistic particles is another. And last but not least, the fact that electrons can travel ballistic, without hitting carbon atoms, for long distances in the micrometer range is another. All these contribute to graphene's success.



Schematic of the device where a nanowire acts as gate for a graphene transistor. Reprinted by permission from Macmillan Publishers Ltd. Nature (2010). doi:10.1038/nature09405

Two years ago I wrote a feature in New Scientist where I focussed on the potential of graphene to replace silicon logic. The piece is now behind a pay wall, but when talking to Andre Geim at the time, a pioneer in the field, he told me that graphene is uniquely suited to scale down to device dimensions impossible to achieve with silicon. Any transistor needs to support an electric current, that is how you read out its status. However, if you shrink the size of a transistor to only a few

nanometers, this electric current will flow across only a small number of atomic bonds. Silicon bonds might not be able to sustain such high current densities. Not so graphene. “The bonds between the carbon atoms in graphene are very strong and can carry exceptionally high currents,” said Geim back then.

When I wrote that New Scientist feature, research into graphene transistors was just about to take off. Now, this almost seems ancient history. The fabrication of graphene has made considerable advances, and transistors with potential speeds up to 100 GHz have been demonstrated. However, large-scale fabrication of graphene devices remains problematic because they often have to rely on the evaporation of other materials directly on graphene, which can lead to degradation.

This is where Xiangfeng Duan and colleagues improve upon. They avoid the conventional top-down approach where the transistor gate (G in the figure), which controls the electric current that flows between source (S) and drain (D) contacts, is deposited directly on the the graphene channel, followed by an etch step that electrically isolates the gate from source and drain. This can damage the gate. Therefore, Duan and colleagues use a nanowire for the gate. They pour a solution with the nanowires on graphene and let the nanowires assume more or less random positions. Once the nanowires are in place the platinum source and drain contacts are evaporated around the nanowire in a single step. This has the benefit that during the deposition process the channel between source and drain is protected by the nanowire directly above.

The performance characteristics of the transistors are convincing. Achievable operation speeds reach 300 GHz. Transconductance, which is a measure of the efficiency of transistor performance, is the highest reported so far. These transistors work very well.

So, what is the problem? Without doubt these transistors are a great achievement. And making individual devices is effortless. But as for other self-assembled devices, such as carbon nanotube transistors, nanowire transistors, a problem has always been placement. It is no problem to have a nanowire assume a random position on a wafer and then making a device around it. But a modern multicore processors contain more than a billion transistors. This is in contrast to the self-assembled devices presented here. Even the reliable, controlled fabrication of 10, 100, or 1,000 transistors on a wafer seems a challenge.

Therfore, even though device characteristics are better than what has been achieved with top-down approaches so far, I cannot see this device design being the one that makes it to the market — if graphene ever makes it to the market that is. I am happy to be proven wrong of course, but part of

graphene's promise has been its two-dimensional character that makes processing so easy. The random or quasi-random placement aspects of the present design just doesn't look as feasible to me. In any case, it won't be easy. A little warning from Geim that he gave me as well: "There have been many contenders that promised to put silicon out of the business, but eventually they all failed miserably."

Source: http://allthatmatters.heber.org/2010/09/01/the-thing-with-graphene-transistors/