THE MICROPROCESSOR AND ITS ARCHITECTURE

The Microprocessor Called the CPU (**central processing unit**).The controlling element in a computer system. The controlling element in a computer system. Controls memory and I/O through connections called buses.

* buses select an I/O or memory device, transfer data between I/O devices or memory and the microprocessor control I/O and memory systems microprocessor, control I/O and memory systems

* Memory and I/O controlled via instructions stored in memory, executed by the stored in memory, executed by the microprocessor.

Microprocessor performs three main tasks:

◦ data transfer between itself and the memory or I/O systems

◦ simple arithmetic and logic operations

◦ program flow via simple decisions

Power of the microprocessor is capability to execute billions of millions of instructions per second from a program or instructions per second from a program or software (**group of instructions**) stored in the memory system.

◦ stored programs make the microprocessor and computer system very powerful devices.

Another powerful feature is the ability to make simple decisions based upon numerical

◦ a microprocessor can decide if a number is zero, positive and so forth positive, and so forth

These decisions allow the microprocessor to modify the program flow so programs to modify the program flow, so programs appear to think through these simple decisions.

The block diagram of 8086 CPU architecture is shown in the figure.

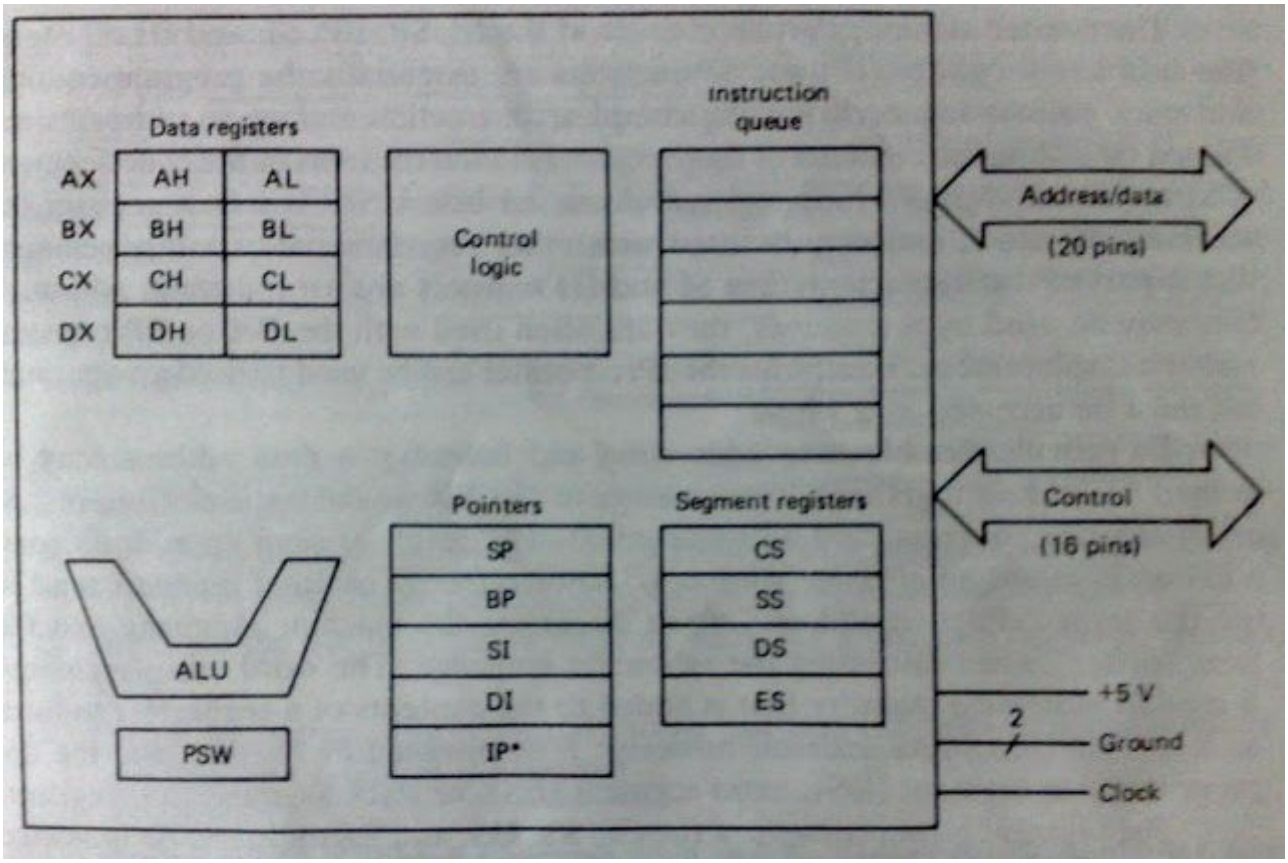

Figure 1.5 8086 CPU Architecture

Data registers- The registers AX, BX, CX and DX are called as the data registers. They are 16 bits wide and can store both the operands and the results. Each of the data registers can either be accessed as a whole or the higher byte and the lower byte can be accessed separately. Example- The whole 16 bits in the register AX can be used together or the higher byte and lower byte can be accessed separately as AH and AL. The registers BX, CX and DX also are used in other functions in addition as being used as the arithmetic registers.
BX is used as a base register in address calculations.
CX is used as an implied counter by some instructions.
DX is used to hold the I/O address during some I/O operations.

Pointer and Index registers- The pointer and index group include the SP, BP, SI, DI and IP. The SP and IP are essentially the stack pointer and instruction pointer. The instruction pointer is also called as the program counter. The complete stack and instruction address is formed by adding the contents of the SP and IP with the contents in CS and SS. BP or base pointer is used to address the beginning of a stack. It is used in combination with other registers and/or with a displacement. SI and DI are the index registers, they are used in combination with the BX or BP and/or a displacement. The SP and BP can be used to store the operands but not the IP. Formation of Effective address (EA)- The data address formed by adding together, a combination of ,BX or BP register contents, SI or DI register contents and a displacement is called as an effective address or offset.

Displacement- The word displacement is used to indicate any quantity that is added to the register contents to form an effective address.

Segment registers- The segment registers are CS, SS, DS and ES. The registers that are used for addressing, SP, BP, SI, DI and IP are 16-bits wide and hence the effective address or offset will be 16 bits wide but the address that is required on the address bus called the physical address is 20 bits wide.

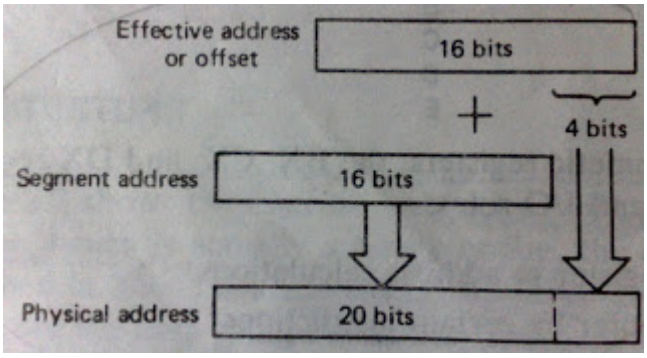

Figure 1.6 Formation of physical address

Formation of physical address- We have seen that the address required on the address bus is 20 bits wide but a problem persists as the effective address formed is only 16 bits wide. Hence the formation of the physical address requires the addition of the contents of the effective address with the contents of any of the segment registers. To generate the extra 4 bits , we have to

append four 0 bits to the right most digit of the number in the segment register. Example if CS = 123A and IP = 341B , the physical address formed by the addition of these two will be

3 4 1 B +

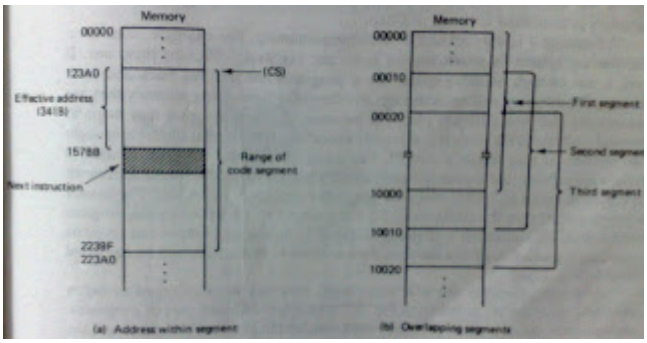

Figure 1.7 overlapping segments

1	2	3	A	0
1	5	7	B	B

Overlapping segments- The use of segment registers divides the memory space into overlapping segments with each segment being 64 Kb wide and beginning at a memory location that is divisible by 16.

Segment address- Contents of a segment register are called as 'segment address'. Beginning segment address - Segment address multiplied by 16 is known as 'beginning segment address'.

Advantages of using segment registers.

1. It allows the memory capacity to be 1Mb even though the individual instructions are only 16 bits wide.
2. It allows the instruction, data and stack portion to be 64Kb wide by facilitating the use of more than one instruction, data and stack segment.
3. Facilitates the program, data and stack to have separate memory portions.
4. Allows the program and its data to be stored in separate parts of memory while execution of the program is performed.

8086 PSW

The 8086 PSW is 16 bits, but only 9 of its bits are used. Each bit of 8086 PSW is called a flag. The flags are divided into two groups, these are conditional flags and control flags. The conditional flags reflect the condition involving a previous instruction execution. The control flags controls the functioning of certain instructions.

Conditional Flags

1. SF (Sign flag)- It is equal to MSB of the result. In 2's compliment a 1 in the MSB shows that the result is a negative number and a 0 in the MSB shows that the result is a non-negative number. Hence the sign flag is used to determine whether the result is positive or negative.

2. ZF (Zero flag) - 1 in the zero flag shows that the result is zero and a 0 in the zero flag shows that the result is a non-zero number.

3. PF (Parity flag) - The PF will become 1 if there are even number of one's in the lower 8-bits of the PSW.

4. CF (Carry flag) - There are two cases here involving addition and subtraction. In addition a carry out of the MSB causes this flag to be set. In subtraction if the MSB borrows then this flag is set.

5. AF (Auxillary carry flag)- In addition the carry out of a bit 3 causes this flag to be set. In subtraction a borrow by bit 3 causes this flah to be set.

6. OF (Overflow flag)- The overflow flag is set when the result is out of range. More specifically, in addition, if there is a carry into the MSB and the MSB has no carry out and in addition, if the MSB needs to borrow and there is no borrow from MSB.

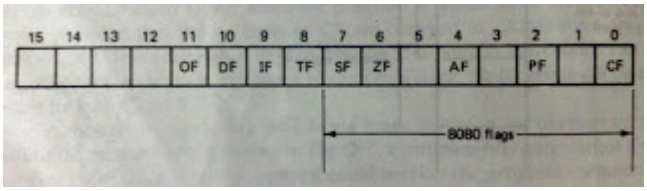

Figure 1.8 8086 PSW

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Control flags

1. DF (Direction flags)- Used by string manipulation instructions. If clear, the string is processed from the beginning, starting with the first element with the lower address If set, the string is processed from the higher address to the lower most address.

2. IF (Interrupt enable flag)- If enabled it helps the CPU to recognize the maskable interrupt else these interrupts are ignored.

3. TF (Trap flag)- If set a trap is executed after each instruction.

Buses

A common group of wires that interconnect components in a computer, Transfer address, data, & control information between microprocessor memory and I/O between microprocessor, memory and I/O.

Three buses exist for this transfer of information: address, data, and control.

Figure 1–10 shows how these buses interconnect various system components.

The address bus requests a memory location from the memory or an I/O location from the I/O from the memory or an I/O location from the I/O devices

◦ if I/O is addressed, the address bus contains a 16-bit I/O address from 0000H through FFFFH.

◦ if memory is addressed the bus contains a memory ◦ if memory is addressed, the bus contains a memory address, varying in width by type of microprocessor.

64-bit extensions to Pentium provide 40 address pins allowing up to 1T byte of memory to be pins, allowing up to 1T byte of memory to be devices.

accessed.

The data bus transfers information between the microprocessor and its memory and I/O address microprocessor and its memory and I/O address space.

Data transfers vary in size, from 8 bits wide to 64 bits wide in various Intel microprocessors.

◦ 8088 has an 8-bit data bus that transfers 8 bits of data at a time

8086 80286 80386SL 80386SX d 80386EX f ◦ 8086, 80286, 80386SL, 80386SX, and 80386EX transfer 16 bits of data 80386DX 80486SX d 80486DX 32 bit ◦ 80386DX, 80486SX, and 80486DX, 32 bits

◦ Pentium through Core2 microprocessors transfer 64 bits of data bits of data.

Advantage of a wider data bus is speed in applications using wide data.

In all Intel microprocessors family members, memory is numbered by byte. Pentium through Core2 microprocessors contain a 64-bit-wide data bus.

Control bus lines select and cause memory or I/O to perform a read or write operation to perform a read or write operation. In most computer systems, there are four control bus connections:

MRDC (**memory read control**)

MWTC (**memory write control**)

IORC (**I/O read control**)( )

IOWC (**I/O write control**).

Over bar indicates the control signal is active low; over bar indicates the control signal is active-low;(active when logic zero appears on control line)

The microprocessor reads a memory location by sending the memory an address through the sending the memory an address through the address bus.

Next, it sends a memory read control signal to cause the memory to read data.

Data read from memory are passed to the microprocessor through the data bus.

Whenever a memory write, I/O write, or I/O read occurs, the same sequence ensues.