

# Temperature Independent Band Gap Reference Voltage Using Regulated Cascode Current Mirror Structure

N.Divya Teja<sup>#1</sup>

#1 B.Tech Project Student, Department of ECE, KL University, Vaddeswaram, Guntur-522502

divyateja255@gmail.com

K.Shreeram<sup>#2</sup>

#2 B.Tech Project Student, Department of ECE, KL University, Vaddeswaram, Guntur-522502

shree.thecoolguy.51.9@gmail.com

G.Rakesh chowdary<sup>#3</sup>, Ch.Srinath Babu<sup>#4</sup>, K.Sneha latha<sup>#5</sup>

#3 Assistant professor, Department of ECE, KLUniversity, Vaddeswaram, Guntur-522502

#4,#5 B.Tech Project Students, Department of ECE, KL University, Vaddeswaram, Guntur-522502

Abstract:

A bandgap reference is a temperature independent voltage reference circuit widely used in integrated circuits usually with an output voltage of 1.25V, close to the theoretical 1.22eV bandgap of silicon at 0k. It is the essential component of an analog-to-digital converter. There are some problems arising from temperature-dependent to power supply rejection ratio when implementing a bandgap reference circuit. The circuit uses a regulated cascode current mirror structure which is the best suitable current mirror for the bandgap reference circuit as it provides medium input and output compliance voltage and very high output resistance. The main design criteria for this project is to achieve PSRR above 60dB and a variation less than 3% resulting from temperature changes between 27°C and 85°C.

Keywords -----bandgap, PSRR, reference voltage, regulated cascode current mirror.

## 1. Introduction

The bandgap reference circuit concept was first published by David Hilbiber in 1964<sup>[1]</sup>. Bob widlar<sup>[2]</sup>, Paul Browkaw<sup>[3]</sup> and others<sup>[4]</sup> followed up with other commercially successful versions. Bandgap circuit with low sensitivity to temperature and supply voltage is commonly required. The best approach is the base emitter junction which consists of a linear combination of base-emitter voltage. We can compensate temperature dependent voltage by adding a positive-TC voltage to a negative-TC voltage. The temperature behavior of a pn junction voltage is described by

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} - \frac{E_g}{KT^2} V_T$$

where  $V_T$  is the thermal voltage. With T at room temperature and  $V_{BE}=750\text{mv}$ ,

$$\frac{\partial V_{BE}}{\partial T} \approx -1.5\text{mv}/^\circ\text{K}$$

The positive-TC voltage comes from the voltage difference between two pn junctions. The fig. 2 shows the reason behind positive-TC voltage.

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T \ln \frac{I_C}{I_S} - V_T \ln \frac{I_C}{nI_S}$$

$$= V_T \ln n$$

where n equals to the current density ratio of Q2 to Q1.

Ideally, adding a positive-TC voltage to a negative-TC voltage can realize a zero temperature coefficient 1.26V at the room temperature. Additionally, the reference voltage is required to be robust to the power supply voltage. An easy way to improve power supply rejection ration (PSRR) is to increase the open loop gain.

## 2. Temperature Independent References

<sup>[5]</sup>Reference voltages or currents that exhibit little dependence on temperature prove essential in many analog circuits. It is interesting to note that, since most process parameters vary with temperature, if a reference is temperature-independent, then it is usually process- independent as well.

We postulate that if two quantities having opposite temperature coefficients' (TCs) are added with proper weighting, the result displays a zero TC. Among various device parameters in semiconductor technologies, the characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative TCs. Even though many parameters of MOS devices have been considered for the task of reference generation, bipolar operation still forms the core of such circuits.

### 2.1 Negative TC-Voltage

The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a pn junction diode exhibits a negative TC. For a bipolar device we can write

$$I_C = I_S \exp(V_{BE}/V_T), \text{ where } V_T = kT/q \dots \dots \dots (1)$$

The saturation currents  $I_S \propto \mu k T n_i^2$ , where  $\mu$  denotes the mobility of minority carriers and  $n_i$  is the intrinsic minority carrier concentration of silicon. The temperature dependence of the quantities is represented as  $\mu \propto \mu_0 T^m$ , where  $m \approx -3/2$ , and  $n_i^2 \propto T^3 \exp[-E_g/(kT)]$ , where  $E_g \approx 1.12\text{eV}$  is the bandgap energy of silicon. Thus,

$$I_S = b T^{(4+m)} \exp(-E_g/kT) \dots \dots \dots (2)$$

where b is a proportionality factor. Writing  $V_{BE} = V_T \ln(I_C/I_S)$ , we can now compute the TC of base-emitter voltage. In taking the derivative of  $V_{BE}$  with respect to T, we must know the behavior of  $I_C$  as a function of temperature. To simplify the analysis, we assume for now that  $I_C$  is held constant. Thus,

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} * \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S} * \frac{\partial I_S}{\partial T} \dots \dots \dots (3)$$

From equation (2)

$$\frac{\partial I_S}{\partial T} = b^{(4+m)} T^{(3+m)} \exp(-E_g/kT) + b T^{(4+m)} \exp(-E_g/kT) (E_g/kT^2) \dots \dots \dots (4)$$

Therefore,

$$\frac{V_T}{I_S} * \frac{\partial I_S}{\partial T} = (4+m) \frac{V_T}{T} + (E_g/kT^2) * V_T \dots \dots \dots (5)$$

With the aid equations (4) and (5), we can write

$$\frac{\partial V_{BE}}{\partial T} = (V_{BE} - (4+m)V_T - \frac{E_g}{q}) / T$$

The above equation gives the temperature coefficient of base-emitter voltage at a given temperature T, revealing dependence on the magnitude of  $V_{BE}$  itself. With  $V_{BE} \approx 750\text{mv}$  and  $T=300^\circ\text{K}$ ,  $\partial V_{BE}/\partial T = 1.5\text{mV}/^\circ\text{K}$ .

From the above equation, we note that the temperature coefficient of  $V_{BE}$  itself depends on the temperature, creating error in constant reference generation if the positive-TC quantity exhibit a constant temperature coefficient.

### B. Positive TC-Voltage

It was recognized in 1964 that if two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature.

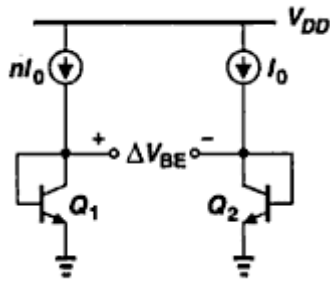


Figure 1 Generation of PTAT voltage

Ligible, then

$$\begin{aligned} \Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{nI_0}{I_{S2}} \\ &= V_T \ln n. \end{aligned}$$

Thus the  $V_{BE}$  difference exhibits a positive temperature coefficient:

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \ln n$$

This TC is independent of the temperature or behavior of the collector currents.

## 3. Circuit Operation Of BGR

### 3.1 Start Up Circuit

The transistors have two states, on and off, when power is provided. In order to make sure the circuit works properly, we need a mechanism which can provide a small current to flow through Op Amp and enable it. This mechanism is also required to be turned off when Op Amp works properly. The start-up circuit consists of transistors, M13-M15. The mechanism works as the following. Since M13 is also in saturation, it provides a sufficient gate voltage for M15 to turn on. When M15 is on, a small current will flow through Op Amp and enable the entire circuit. Furthermore<sup>[6]</sup>, M14 will turn on and sink all the current from M13 and disable M15. Then the start-up circuit is disabled.

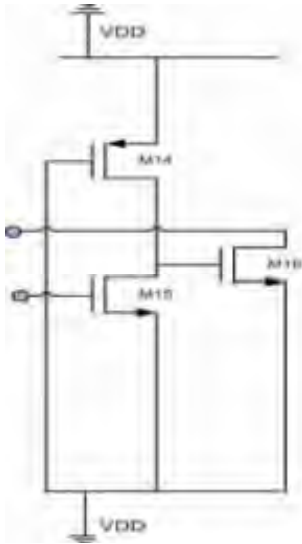


Fig 2 Start Up Circuit

### 3.2 Differential Amplifier

In the circuit depicted in Fig 3, we need to force node X and Y to have the same voltage. We use an operational amplifier for this purpose. It is composed by the common-source stages with diode-connected loads. In order to increase the gain, we stack two pmos transistors into it and its gain can be expressed as

$$A_V = g_{m10} [(g_{m8} + g_{mb8})r_{o6}r_{o8} // r_{o10}]$$

Its output provides a bias for the entire circuits, and a feedback loop is formed. Therefore<sup>[7]</sup>, this bias voltage ideally provides a constant  $V_{gs}$  for the pmos transistors and a constant current can be obtained.

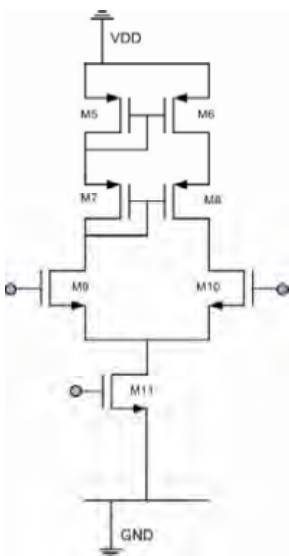


Fig 3 Basic Differential Amplifier stage

### 3.3. Bandgap

Fig. 4 [8][9] shows the basic bandgap circuit. Because of high gain Op Amp, the voltage at node X and Y is forced to be equal.

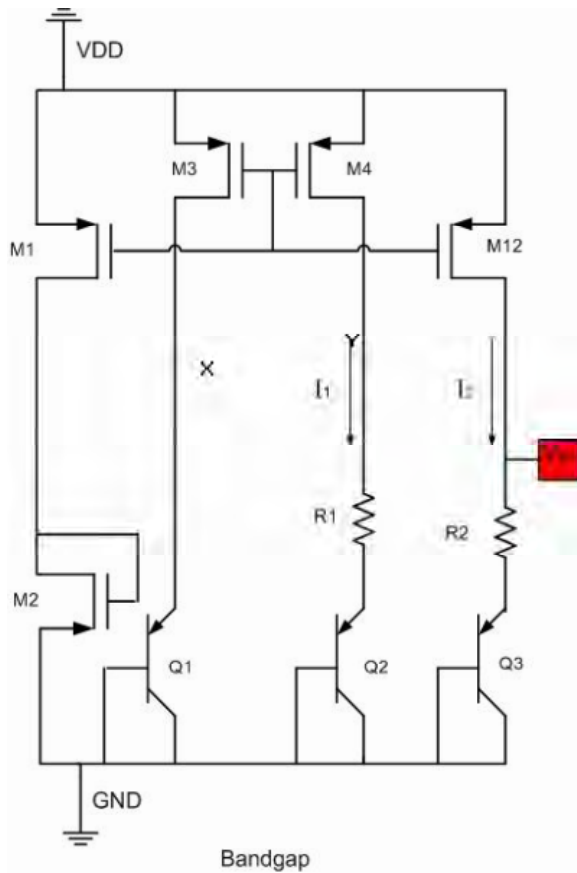


Figure 4 Basic bandgap circuit

$$V_X = V_Y = V_{BE1} = V_{BE2} + I_1 \times R_1 \text{ where}$$

$$V_{BE} = V_T \ln \left( \frac{I_C}{I_S} \right)$$

Therefore,

$$V_{BE1} - V_{BE2} = V_T \ln n = I_1 \times R_1$$

The voltage difference between the two pn junctions is the positive-TC voltage. The current across R1 equals to  $V_T \frac{\ln(n)}{R_1}$  which is called the proportional to absolute temperature (PTAT) current. A PTAT current can be copied from the current mirror and can be adjusted by changing the width of M12 or the resistance of R1. Adding a positive-TC voltage  $I_2 R_2$  to a base-emitter voltage, the negative-TC voltage, can achieve a temperature independent voltage. The ideally reference voltage equals

$$V_{ref} = V_{BE3} + V_T \frac{\ln(n)}{R_1} R_2$$

The n is usually chosen to be eight for the layout purpose.

#### 4. Regulated Cascode CM Structure

The well desired property of good current mirror is its high output resistance. An improvement in Wilson Current Mirror structure<sup>[10]</sup> can be made if somehow its output resistance is increased. This can be achieved by using negative current feedback circuit. The resulted circuit is shown in Fig. 5

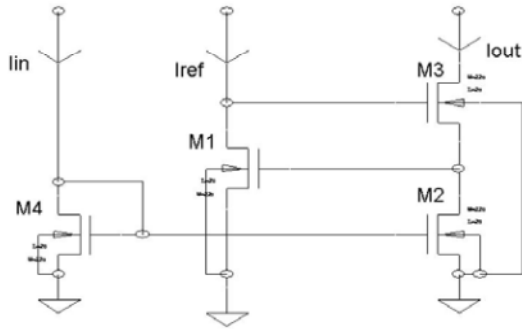


Figure 5 Regulated Cascode CM

The output compliance voltage for this structure is given as

$$V_{out} = \sqrt{\frac{2I_{out}}{\beta_2}} + \sqrt{\frac{2I_{out}}{\beta_3}}$$

The output resistance for this structure is given as

$$r_{out} \approx r_{ds2}g_{m3}r_{ds3}g_{m1}r_{ds1}$$

So this structure achieves an output resistance on the order of  $g_m^2 r_{ds}^3$

The output characteristic of this structure is shown in Fig. 6

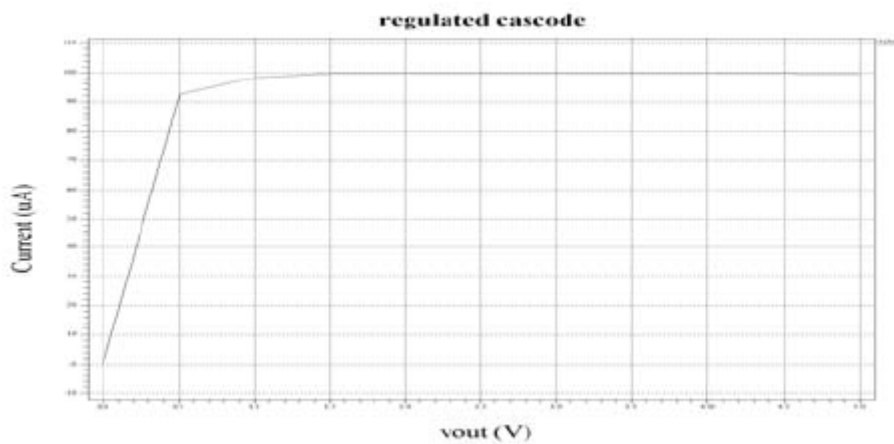
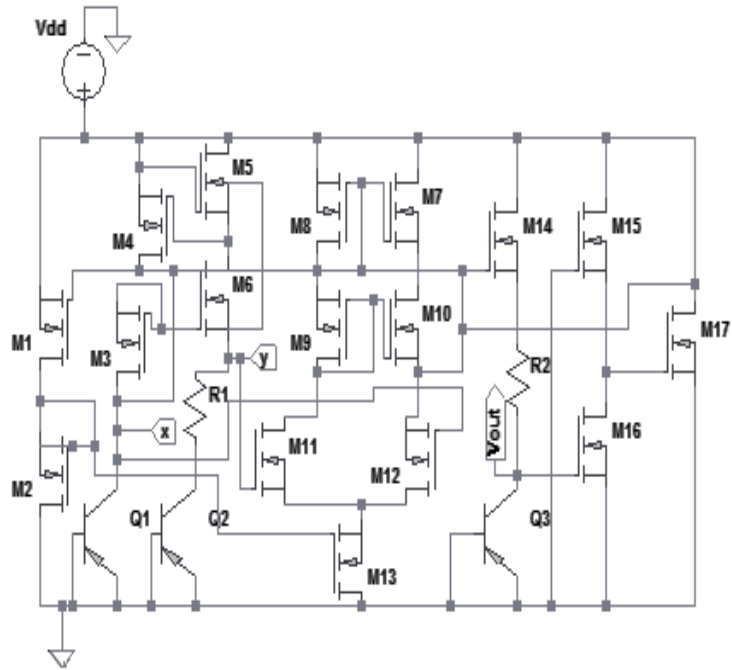


Figure 6 Output characteristics for Regulated Cascode CM

As can be seen from the above Fig 6, output compliance voltage for this structure is 1.5V. Also in saturation mode, output current is constant as it should be ideally.

Hence, we use the Regulated Cascode CM instead of simple CM in the bandgap circuit. But the CM does not influence the output of the bandgap circuit or the temperature independency of the circuit. The final circuit would be given as



**5. Simulation**

The reference voltage is required to be 1.26V at room temperature. The relationship between reference voltage and base-emitter voltage is given by

$$V_{ref} = V_{BE3} + I_2 R_2$$

The base-emitter voltage is 0.75V at 25°C. We can set the PTAT current going through R<sub>2</sub> to be 54µA. Therefore, from the above equation, the resistance of R<sub>2</sub> can be determined by

$$\text{—————} \approx 9.4K$$

For Cadence<sup>[11]</sup> simulation, the appropriate R<sub>2</sub> is 9.37K. Fig. 6 shows the reference voltage changes with temperature ranging from 27°C to 85°C and 10% supply voltage variation. The reference voltage changes around 7.24mV. The V<sub>ref</sub> is very low sensitive to the changes of the temperature. The power supply rejection ratio is shown in Fig.6. From Fig.6, the circuit of the BGR is robust to the power supply when the temperature changes from 27°C to 56°C.

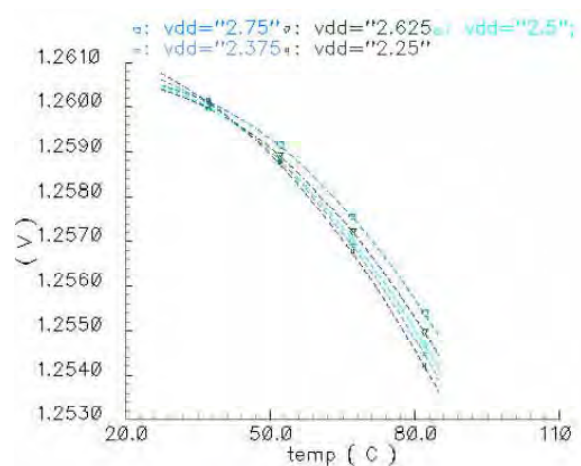


Fig 7 Temperature dependence of bandgap output voltage

The power supply rejection ratio is shown in Fig 7 and from the figure, it is clear that the circuit of the BGR is robust to the power supply when the temperature changes from 27°C to 56°C. The exact PSRR and reference voltages for certain values are depicted in the Table 1.

Table 1 Outcomes of PSRR and reference voltage at certain temperature.

Temperature(°C)	Voltage Variation
27°C	376.707μV
55.6 °C	499.067μV
85 °C	1.25189mV

## 6. Conclusion

A design using bandgap core circuit with Op amp and start-up circuit is presented and simulated. The overall performance of the bandgap reference circuit is summarized in the table 2.

Table 2 Summary of performance

Parameter	Measured
Supply voltage range	2.5V±10%
Temperature Range	27°C to 87 °C
V <sub>REF</sub>	1.26079V~1.25365V
PSRR	>52dB
Power Consumption	0.5W

Comparisons with other design are shown in table 3.

Table 3(a) Comparison between different designs

	Design[12]	Our Design
Supply Voltage	1V	2.5V
PSRR	>40dB	>60dB
Temperature Variation	1.2mV~5.4Mv (-20 °C~50°C)	7mV≈0.58% (27°C~85°C)

Table 3(b) Comparison between different designs

	Design[13]	Our Design
Supply Voltage	2V	2.5V
Temperature Variation	<0.1% (-30°C~125°C)	7mV≈0.58% (27°C~85°C)
Power Consumption	2.2mW	0.5mW

## Acknowledgments

The authors would like to thank the management of KL University, Vaddeswaram for excellent encouragement during the tenure of work.



## References

- [1] Hilbiber, D.F. (1964), "A new semiconductor voltage standard", *1964 International Solid-State Circuits Conference: Digest of Technical Papers* 2:32-33.
- [2] Widlar, Robert J. (February 1971), "New Developments in IC Voltage Regulators", *IEEE Journal of Solid-State Circuits* 6 (1): 2–7.
- [3] Brokaw, Paul (December 1974), "A simple three-terminal IC bandgap reference", *IEEE Journal of Solid-State Circuits* 9 (6): 388–393.
- [4] Banba, H.; Shiga, H.; Umezawa, A.; Miyaba, T.; Tanzawa, T.; Atsumi, S.; Sakui, K. (May 1999), "A CMOS bandgap reference circuit with sub-1-V operation", *IEEE Journal of Solid-State Circuits* 34 (5): 670–674.
- [5] David Jones "Analog Integrated Circuit Design.
- [6] K. Lasanen, V. Korkala, "Design of a 1-V low power CMOS bandgap reference based on resistive subdivision", IEEE.
- [7] T. L. Brooks and A. L. Westwick, "A low-power differential CMOS bandgap reference," in *ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 248–249.
- [8] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGRAW-Hill, 2000.
- [9] M. Ismail and T. Fiez, "Analog VLSI Signal and Information Processing," New York: Tata McGraw-Hill 2002.
- [10] P.E. Allen and D. R. Holberg, "CMOS analog circuit design," New York: Oxford University Press, 2002.
- [11] S. S. Rajput and S. S. Janmuar, "A high performance current mirror for low voltage designs," Proc. APCCAS-2000/IEEE, Tianjin pp. 170-173, China, Dec 2000.
- [12] I. M. Filanovsky, "Current Mirrors with Limiting of Linear Dynamic Range," University of Alberta, Edmonton, Alberta, Canada, T6G 2E1.
- [13] E. SACKINGER and W.GUGGENBUHL, "A versatile building block: the CMOS differential difference amplifier," IEEE SC-22, (2), PP. 287-294.
- [14] D. A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons, Inc., New York, 1997.
- [15] G. R. Wilson, "A Monolithic Junction FET-npn Operational Amplifier," IEEE J. Solid-State Circuits, Vol. SC-3, No. 5, pp.341-348, Dec. 1968.
- [16] Z. Wang, "Analytical determination of output resistance and DC matching errors in MOS current mirrors," IEEE PROCEEDINGS, Vol. 137, Pt. G, No. 5, OCTOBER 1990.