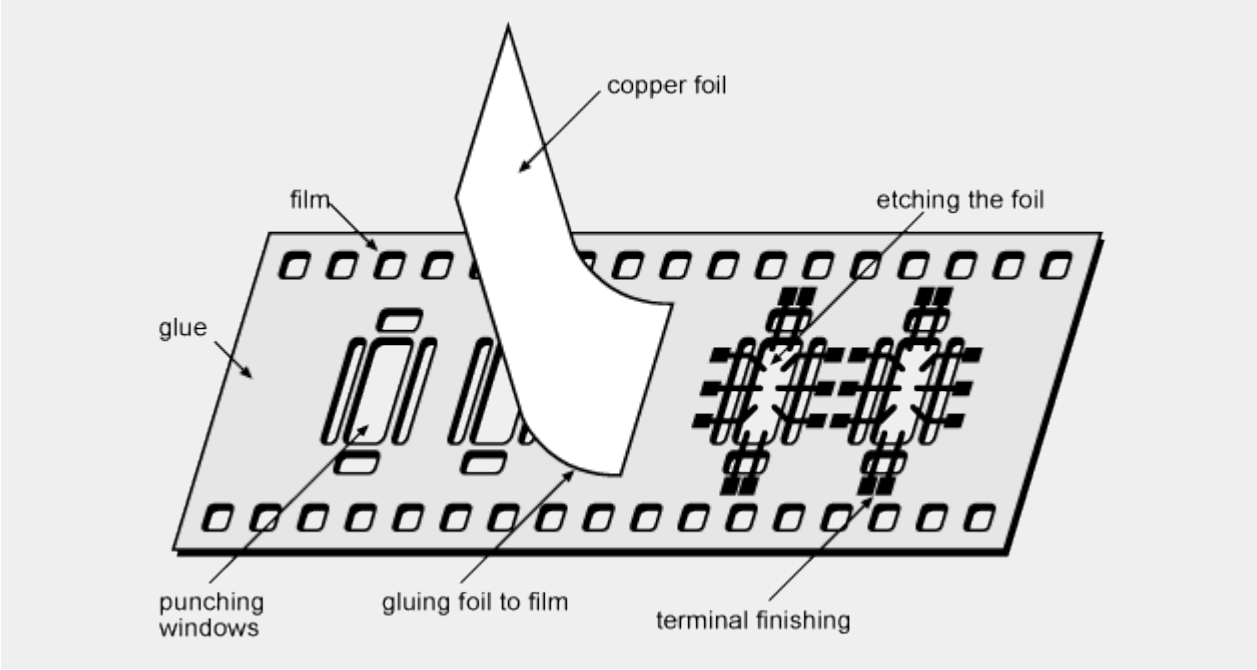
Tape Automated Bonding

Introduction

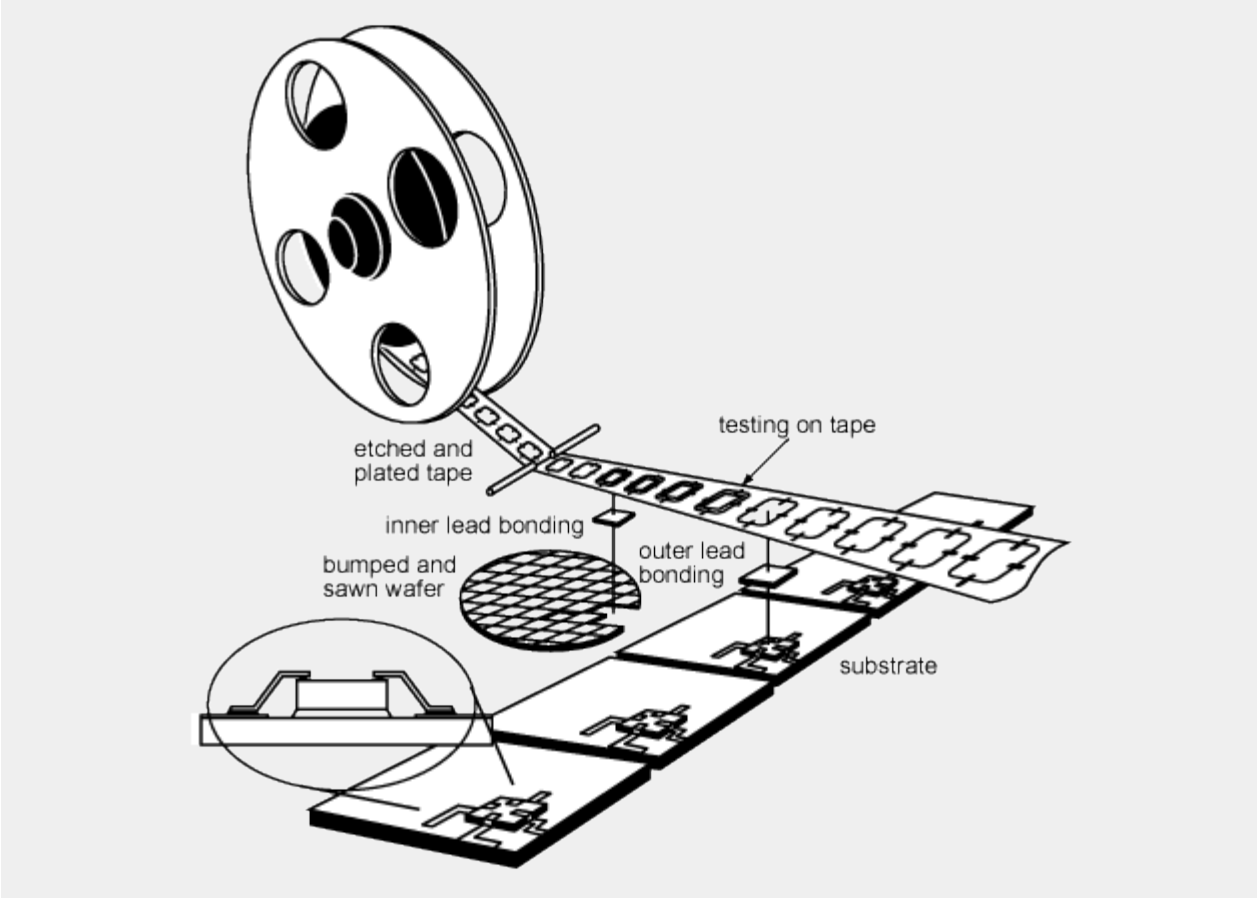
TAB evolved from the miniMOD project begun at General Electric in 1965, and the term ‘Tape Automated Bonding’ was coined by Gerard Dehaine of Honeywell Bull in 1971. The first process used etched copper tape laminated to a sprocketed 35mm polyimide film (Figure 1) and an automated reel-to-reel assembly system (Figure 2).

Figure 1: Progressive build-up of a TAB tape



The inner section of the copper tape was attached by thermocompression bonding to gold bumps on the die pads, and the outer section soldered or welded to the board. Both were simultaneous ‘gang bonding’ operations, in contrast to wire bonding, which was then slow and operator-dependent.

Figure 2: Schematic of a Farco ‘bumped’ wafer TAB processing machine



TAB was thus attractive to high volume manufacturers because it was automated, and in the 1970s there were two distinct markets:

- In the USA, for bonding TTL logic devices in plastic DIP packages (Fairchild, Motorola, National Semiconductor and Texas Instruments)
- In Japan and Europe, in consumer applications such as hearing aids, watches, cameras and calculators, where the flexibility of the laminate was an advantage.

However, TAB requires special silicon and tape tooling, and the development of high-speed automated bonders in the late 1970s and early 1980s resulted in most volume applications being converted back to the more flexible conventional wire bond processes.

More recently there has been renewed interest in TAB, on the grounds of technical advantage over wire bonding:

- TAB has an inherently low profile (50–100µm above the chip), and is capable of bonding to 50×50µm pads with 100µm centre line spacing. This makes it more immediately suitable than conventional wire bonding (especially ball bonding) for SMART cards, watches, credit card calculators and read/write head circuitry
- TAB has better high frequency characteristics, with reactance values which are both low and constant (Table 1)

- TAB has lower electrical and thermal resistances because of the larger cross-sectional area of the leads
- TAB has stronger leads, which are more resistant to mould sweep
- TAB offers the ability to pre-test and burn in components, offering a potential strategy for supplying Known Good Die for MCM applications
- TAB has a greater potential for reel-to-reel automation

Table 1: Electrical performance comparison of wire bonding and TAB

parameter	wire bond	TAB
resistance	0.38mΩ	0.31mΩ
inductance	10nH	6.7nH
capacitance	0.21pF	0.11pF

A number of materials developments have contributed to the growth of TAB:

- Polyimide films with better dimensional stability, elastic modulus, TCE, thermal shrinkage and moisture absorption properties than the original Kapton® film
- Copper TAB tape alloys with better properties for fine pitch, high lead count applications
- The development of tapes with a second metal layer, providing a ground plane for improved electrical performance. One manufacturer has even produced a dual power plane 3-layer tape.

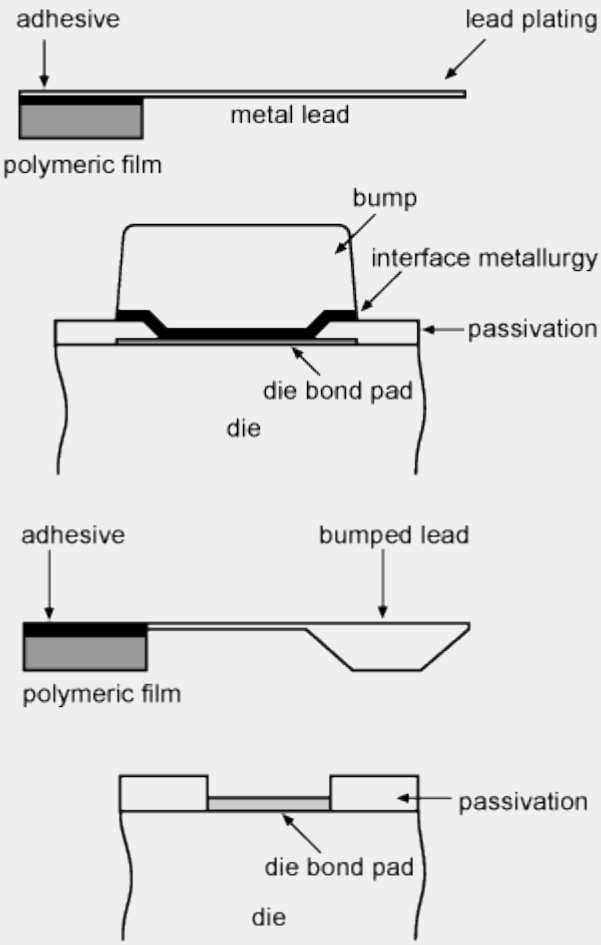
However, one aspect which has adversely affected the uptake of TAB is the comparative lack of agreement on physical standards in the areas of inner lead bond and outer lead bond footprints and the interface with test pad sockets.

Chip bumping and TAB tape

Although Hewlett-Packard have patented a bump-less TAB process, a bump on either the die pad or the cantilever TAB beam (Figure 3) is generally needed in order to be able to connect the two without the beam touching the die surface. There are three bumping options:

- Conventional wafer bumping, typically of gold, although there has been some research on nickel bumps
- Transferred bump TAB, developed by Matsushitu, where bumps are formed on a substrate and transferred to the inner leads on the tape.
- Plated TAB tape, as used by NTT, where the tape leads are gold plated, eliminating the need for chip bumps

Figure 3: Basic TAB principles of bumped chip (left) and bumped lead (right)



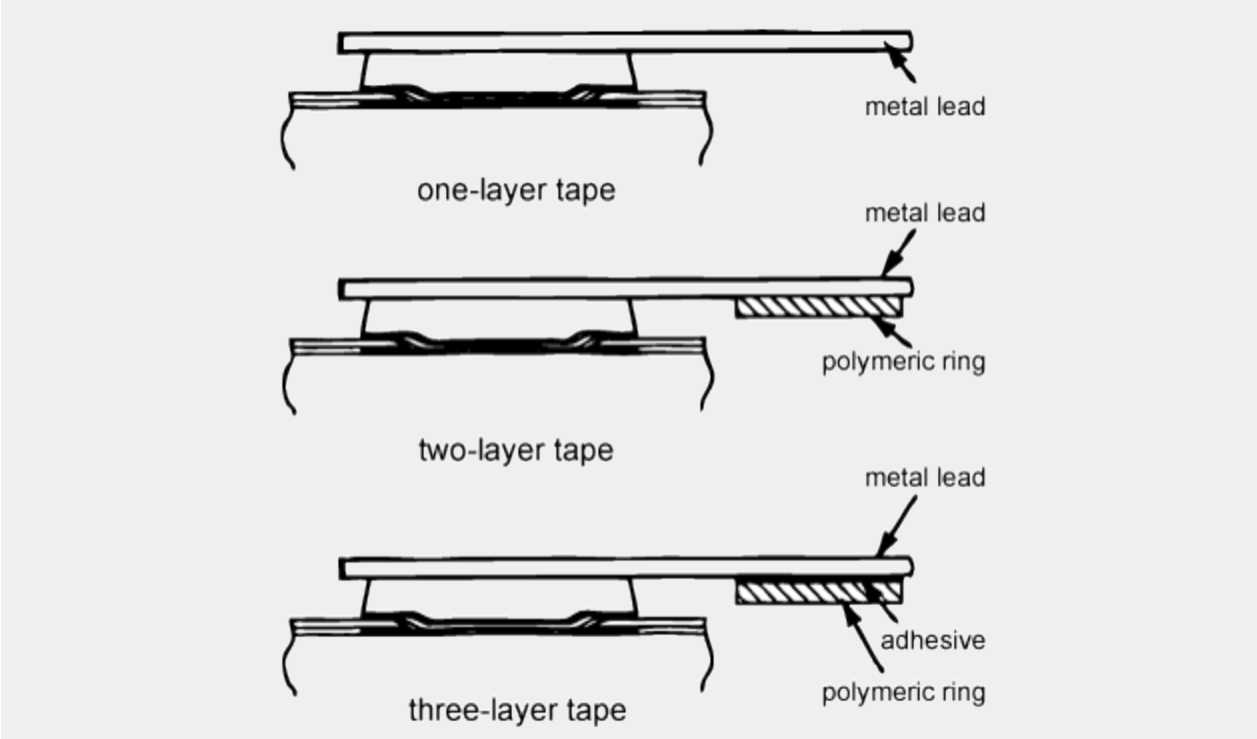
Whilst the bump may be placed on either surface, and wafer bumping is expensive, Vardaman points out that creating a bump on the pad enables the manufacturer to include a passivation layer to help seal and protect the chip from the environment.

One limitation for low volume applications is that bumping the die has previously been a process applied to a whole wafer. However, a single chip electroless nickel bumping process developed by the Technical University of Berlin does not require sputtering or masking, and can be applied to die of 3.5mm side or above.

There are three generic constructions used in common TAB tapes (Figure 4):

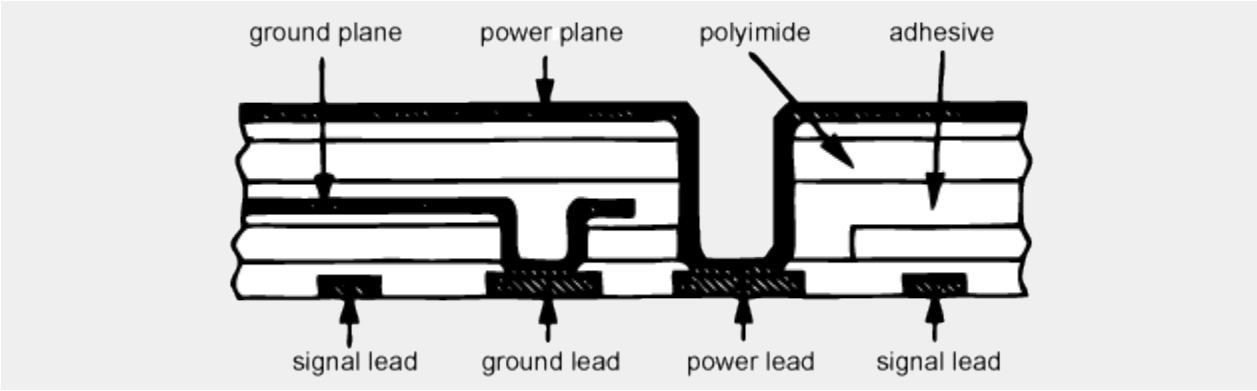
- All-metal tape, which is a single layer of copper without a dielectric layer. Gold plated copper tape is used by NEC for the SX3 super computer
- Two-layer tape, where copper is directly laminated to polyimide
- Three-layer tape, with copper and polyimide but a separate adhesive layer

Figure 4: Differences between 1/2/3-layer TAB tape



‘Ground plane’ tape has one or more extra metal planes to provide controlled impedance (Figure 5). This considerably improves cross-talk and switching noise with terminated systems, but is not so effective for circuits with high input impedance drivers, such as most CMOS applications.

Figure 5: Schematic cross-section of three-level TAB tape



Inner lead bonding

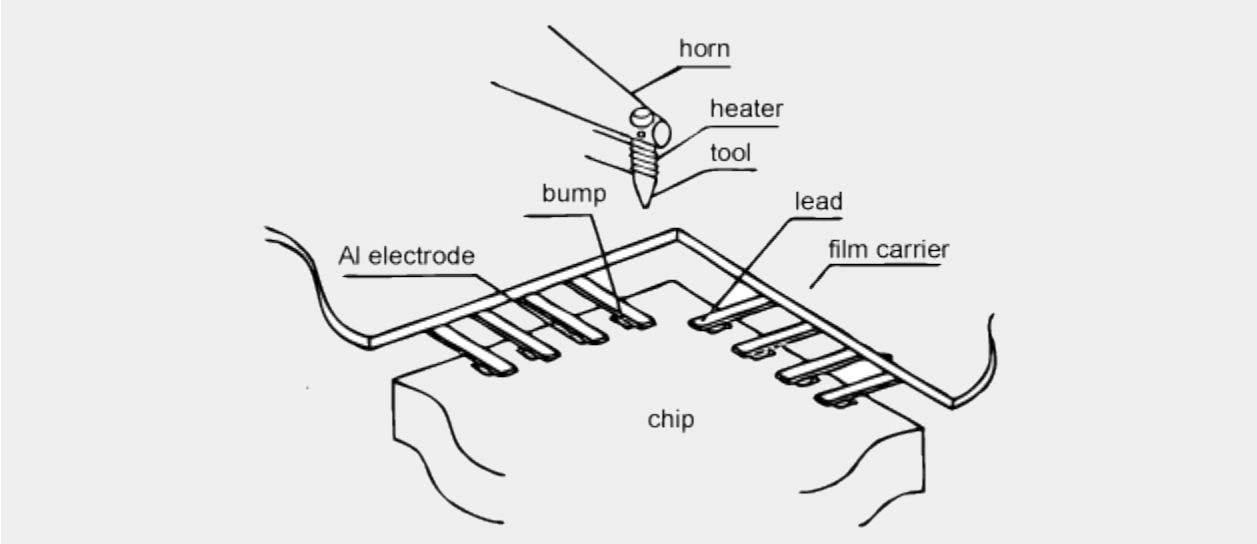
The original TAB inner lead bonding (ILB) process was thermocompression gang bonding. The chip is placed beneath the window of a TAB tape, the bond pads are aligned with the lead fingers, and a thermode used to apply heat (3–400ºC) and pressure (15,000psi) simultaneously to all the leads, a bonding process which takes 1–

5s. This high speed assembly process gives constant throughput which is independent of lead count.

However, thermocompression gang bonding exerts a comparatively high force per bond and needs excellent die and tape planarity, with minimal variation in tape or bump height. As die sizes and lead counts increase, it becomes difficult to obtain the tight planarity tolerance needed: if a bond pad has even a few µm variation from side to side, uneven forces will be applied, resulting in poor bonding.

'Single point TAB' overcomes these problems, giving higher yields and more consistent bonds, albeit more slowly. In the thermosonic bonding variant, individual leads are bonded in sequence at around 10 leads per second, using pressure and ultrasonic vibration, as with wire bonding. This single point bonding process is used by Matsushita in 'transferred bump TAB' for bonding to the die pad (Figure 6).

Figure 6: Single-tool method for TAB bonding



Equipment has been developed using high speed wire bonding mechanisms, with die to tape alignment under computer control and pattern recognition to determine the exact position of bond pad, and which will operate with minimal set-up and device change-over times. This approach has allowed TAB to be extended towards 1,000 leads, with die of 16mm square.

An alternative, which reduces the thermal and mechanical stresses of TAB bonding, is laser TAB processing, where the leads are aligned to pads on the chip and a focused neodymium/YAG laser beam positioned over the chip and pulsed once. Advantages of this method are that:

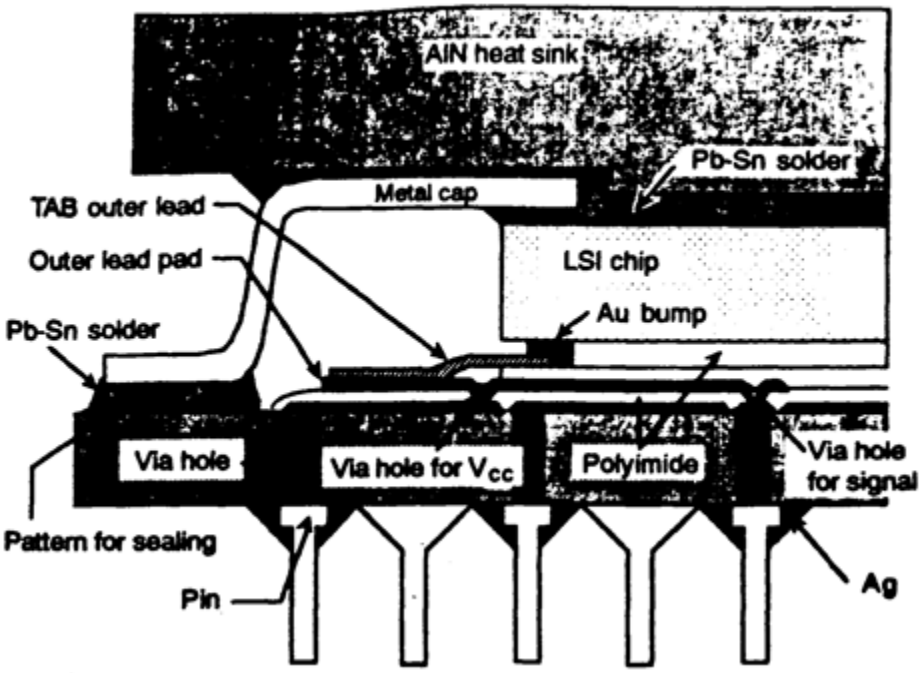
- Bonding speeds obtainable are considerably higher (Crowley claimed 65 leads per second in 1991)
- The lead pitch is limited by the laser beam diameter rather than the tool size or bonding pressure, allowing TAB leads of 30µm on 75µm pitch
- The bond pads can be in an area array format, rather than on the periphery

Inner lead bonding has to be considered in conjunction with die support, and in many cases silver-loaded adhesive is used to provide a thermal and electrical path to a substrate. tab devices usually have a large contact area, requiring a thin, even spread of

adhesive, obtained by depositing a pattern of dots and/or lines on the mounting area. As with conventional die bonding, the dispensed pattern of adhesive is designed so that, when the device is placed, the adhesive provides the desired bond line with no trapped air and little excess material at the periphery.

TAB packages have also been used by companies such as Fujitsu as the basis of high dissipation assemblies, where a device is first bonded to the interconnect and then soldered on its reverse to a heat sink (Figure 7).

Figure 7: Fujitsu single chip package cross-section



Outer lead bonding

TAB outer lead bonds (OLB) are of copper with a final metallisation of tin or gold, and the pads to which they are bonded are normally coated with eutectic tin-lead solder. In order to overcome potential problems over lack of co-planarity, the soldering method normally adopted is hot bar soldering, which applies both heat and light pressure to all the leads simultaneously. An extended pulse of heating current is passed through a non-wetting electrode, which is held in contact with the leads until the resulting joints have solidified.

The mechanical stability and thermal cycling behaviour of the outer lead bond are determined by the ductility of the copper lead and the geometry of the solder joint formed during the OLB process. Whilst sufficient solder is needed, the solder thickness must be reduced in fine pitch applications in order to avoid solder bridges. DiFranchesco also pointed out that the mechanical parameters of the lead material itself are important: ‘Uncontrolled copper hardness defeats lead forming and makes outer lead bonding a very difficult task’.

Gold plating on the outer lead contact area can improve performance. Zakel investigated both the changes in material and the results from mechanical pull tests, and found that 0.8µm gold thickness gave the best results because of better solder fillet formation:

- Increasing the gold thickness may lead to intermetallic compounds in the solder ($AuSn_4$, $AuSn_2$ and AuSn) which form needle-like crystals, causing embrittlement and reducing ductility
- With less gold, failure resulted from the reduction in the lead thickness due to the formation of copper-tin intermetallics

Soldering is not the only OLB option: bonding down to 80µm pitch has also been carried out using anisotropically conducting adhesive. The Casio material used consists of conductive particles with plastic cores which are plated with nickel gold, to which are applied smaller particles coated with a very thin insulating film. Combined in an epoxy binder, the material is thermocompression bonded to the indium tin oxide electrode on the LCD substrate, breaking down the insulating film in the direction of applied pressure to make an electrical contact.

Protection and burn-in

As with Chip-On-Board assemblies, TAB parts may be protected by covering the entire top surface of the die and lead-frame with a polymer formulated to have a low ionic content and high resistance to water absorption to prevent corrosion of the aluminium die interconnect. Because the TAB connection is robust, and has a lower profile than wire bonds, the coating can be both thinner and have a lower profile.

A reduced level of protection may be provided by:

- Covering just the top surface of the die
- Placing a line of epoxy only over the TAB bond areas on the die
- Omitting the secondary protection entirely, increasing instead the thickness of die passivation

In these cases, a further coating may be required to give an appropriate level of protection to the completed module.

Smart recommends that ‘if thermal performance permits, a fully encapsulated die offers the module manufacturer the greatest protection during assembly. The use of non-packaged ICs forces the module manufacturer to inspect for and eliminate scratches or signs of ionic or other contamination.’

From the application point of view, TAB has the major advantage that it may be tested before assembly, with fully functional, full frequency testing and burn-in to reduce infant mortality. This is particularly important for the MCM manufacturer, where yield affects are additive.

Source : http://www.ami.ac.uk/courses/topics/0258_tab/index.html