SYNCHRONIZED UJT OSCILLATOR

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A synchronized UJT triggering circuit is as shown in figure below. The diodes rectify the input ac to dc, resistor R_d lowers V_{dc} to a suitable value for the zener diode and UJT. The zener diode 'Z' functions to clip the rectified voltage to a standard level V_Z which remains constant except near $V_{dc}=0$. This voltage V_Z is applied to the charging RC circuit. The capacitor 'C' charges at a rate determined by the RC time constant. When the capacitor reaches the peak point V_P the UJT starts conducting and capacitor discharges through the primary of the pulse transformer. As the current through the primary is in the form of a pulse the secondary windings have pulse voltages at the output. The pulses at the two secondaries feed SCRs in phase. As the zener voltage V_Z goes to zero at the end of each half cycle the synchronization of the trigger circuit with the supply voltage across the SCRs is archived, small variations in supply voltage and frequency are not going to effect the circuit operation. In case the resistor 'R' is reduced so that the capacitor voltage reaches UJT threshold voltage twice in each half cycle there will be two pulses in each half cycle with one pulse becoming redundant.

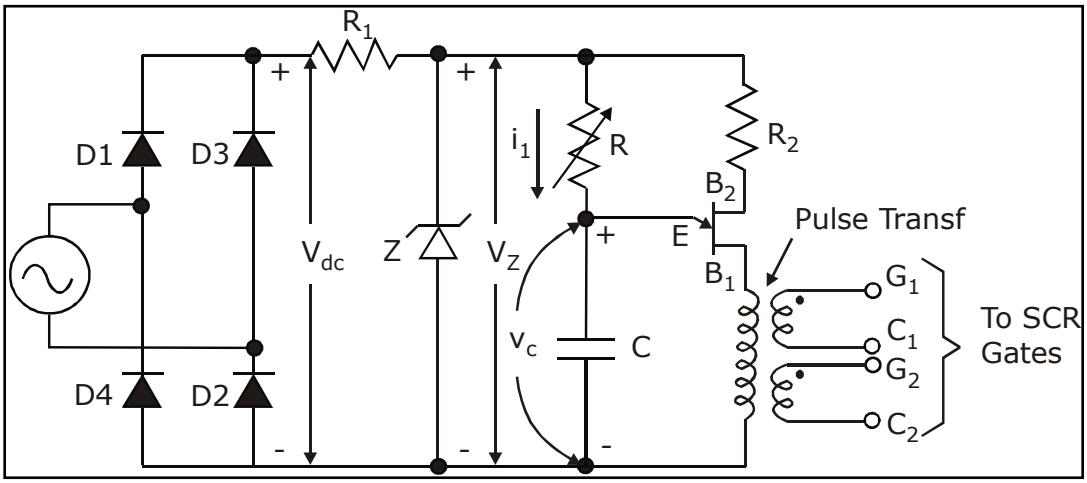

Fig.3.14: Synchronized UJT trigger circuit

Digital Firing Circuit

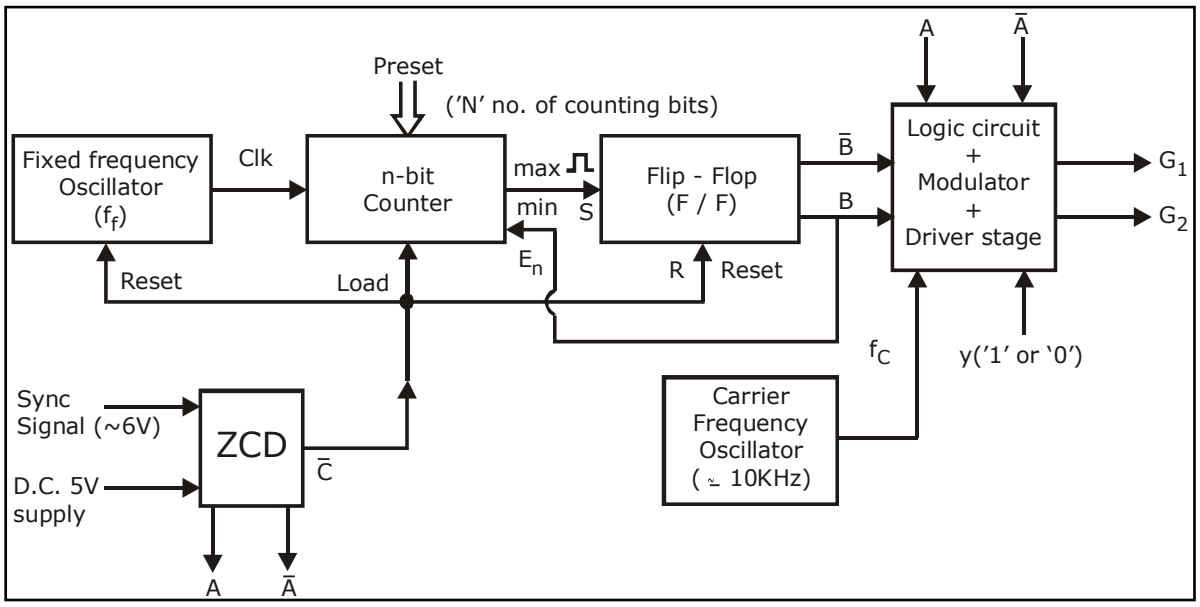

Fig.3.15: Block diagram of digital firing circuit

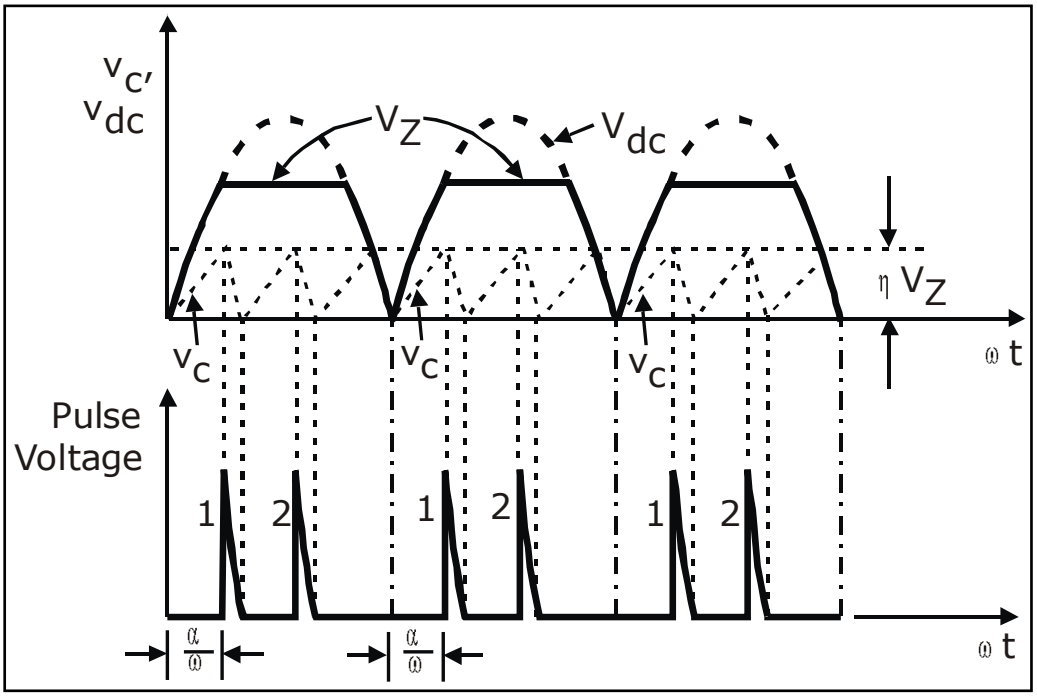

Fig.3.16: Generation of output pulses for the synchronized UJT trigger circuit

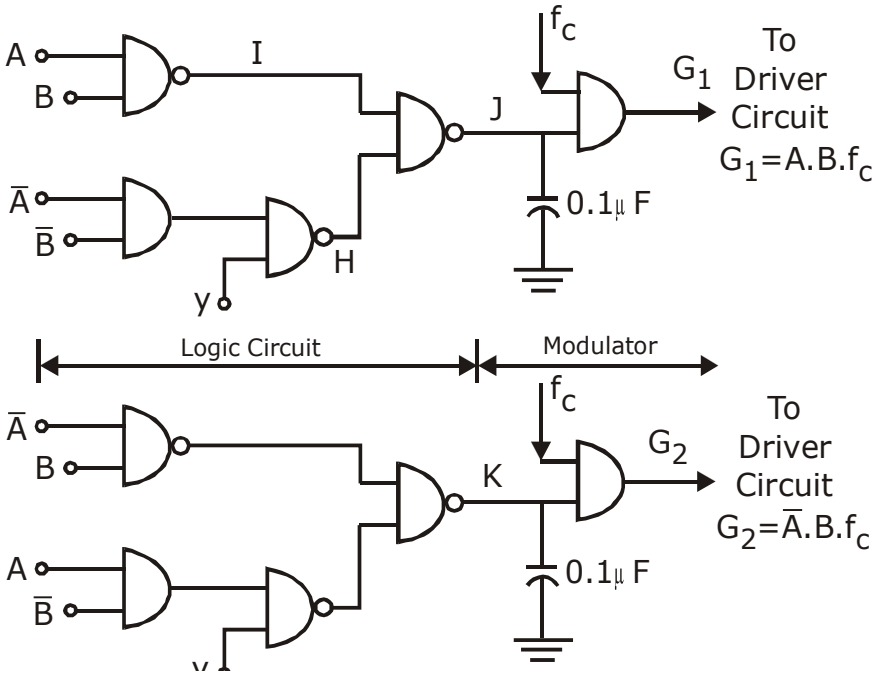

Fig.3.17: Logic circuit, Carrier Modulator

The digital firing scheme is as shown in the above figure. It constitutes a pre-settable counter, oscillator, zero crossing detection, flip-flop and a logic control unit with NAND and AND function.

Oscillator: The oscillator generates the clock required for the counter. The frequency of the clock is say f_C. In order to cover the entire range of firing angle that is from 0^0 to 180^0, a n-bit counter is required for obtaining 2^n rectangular pulses in a half cycle of ac source. Therefore 4-bit counter is used, we obtain sixteen pulses in a half cycle of ac source.

Zero Crossing Detector: The zero crossing detector gives a short pulse whenever the input ac signal goes through zeroes. The ZCD output is used to reset the counter, oscillator and flip-flops for getting correct pulses at zero crossing point in each half cycle, a low voltage synchronized signal is used.

Counter: The counter is a pre-settable n-bit counter. It counts at the rate of f_C pulses/second. In order to cover the entire range of firing angle from 0 to 180^0 , the n-bit counter is required for obtaining 2^n rectangular pulses in a half cycle.

Example: If 4-bit counter is used there will be sixteen pulses / half cycle duration. The counter is used in the down counting mode. As soon as the synchronized signal crosses zero, the load and enable become high and low respectively and the counter starts counting the clock pulses in the down mode from the maximum value to the pre-set value 'N'. 'N' is the binary equivalent of the control signal. once the counter reaches the preset value 'N' counter overflow signal goes high. The counter overflow signal is processed to trigger the Thyristors. Thus by varying the preset input one can control the firing angle of Thyristors. The value of firing angle α can be calculated from the following equation

$$\alpha = \left(\frac{2^n - N}{2^n}\right)180^0 = \left(1 - \frac{N}{16}\right)180^0 \quad \text{for } n = 4$$

Modified R-S Flip-Flop: The reset input terminal of flip-flop is connected to the output of ZCD and set is connected to output of counter. The pulse goes low at each zero crossing of the ac signal. A low value of ZCD output resets the B-bar to 1 and B to 0.

A high output of the counter sets B-bar to 0 and B to 1. This state of the flip-flop is latched till the next zero crossing of the synchronized signal. The output terminal B of flip-flop is connected with enable pin of counter. A high at enable 'EN' of counter stops counting till the next zero crossing.

Input		***Output***		***Remarks***
R	***S***	***B***	***B-bar***	
1	***1***	***1***	***0***	
0	***1***	***1***	***0***	***Set***
0	***0***	***0***	***1***	***Reset***
1	***0***	***0***	***1***	***Last Stage***
1	***1***	***1***	***0***	

Truth Table of Modified R-S Flip-Flop

Logic Circuit, Modulation and Driver Stage: The output of the flip-flop and pulses A and A-bar of ZCD are applied to the logic circuit. The logic variable Y equal to zero or one enables to select the firing pulse duration from α to π or α