

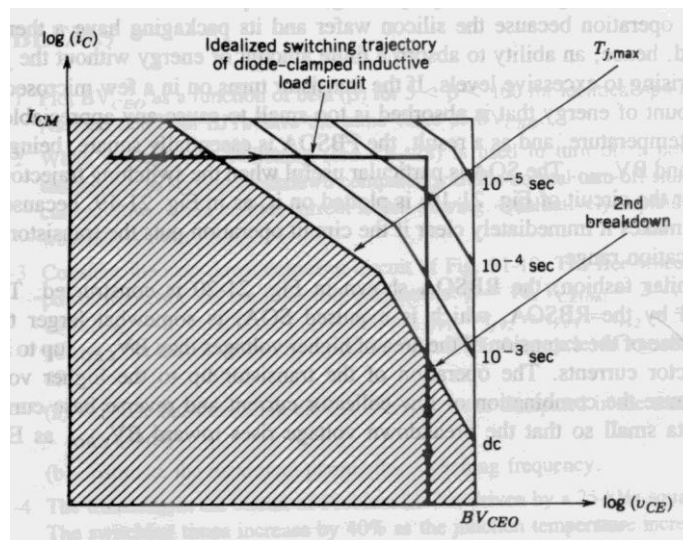
SWITCHING LIMITS

1. Second Breakdown

It is a destructive phenomenon that results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient the excessive localized heating may damage the transistor. Thus secondary breakdown is caused by a localized thermal runaway. The SB occurs at certain combinations of voltage, current and time. Since time is involved, the secondary breakdown is basically an energy dependent phenomenon.

2. Forward Biased Safe Operating Area FBSOA

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturer usually provides the FBSOA curves under specified test conditions. FBSOA indicates the $I_c - V_{ce}$ limits of the transistor and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.



The dc FBSOA is shown as shaded area and the expansion of the area for pulsed operation of the BJT with shorter switching times which leads to larger FBSOA. The second breakdown boundary represents the maximum permissible combinations of voltage and current without getting into the region of $i_c - v_{ce}$ plane where second breakdown may occur. The final portion of the boundary of the FBSOA is breakdown voltage limit BV_{CEO} .

3. Reverse Biased Safe Operating Area RBSOA

During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-emitter junction reverse biased. The collector emitter voltage must be held to a safe level at or below a specified value of collector current. The manufacturer provide

$I_c - V_{ce}$ limits during reverse-biased turn off as reverse biased safe area (RBSOA).

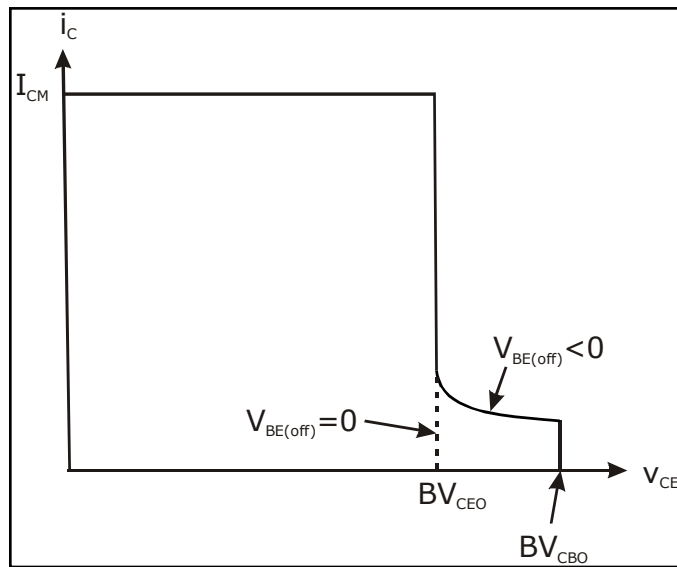


Fig.2.8: RBSOA of a Power BJT

The area encompassed by the RBSOA is somewhat larger than FBSOA because of the extension of the area of higher voltages than BV_{CEO} upto BV_{CBO} at low collector currents.

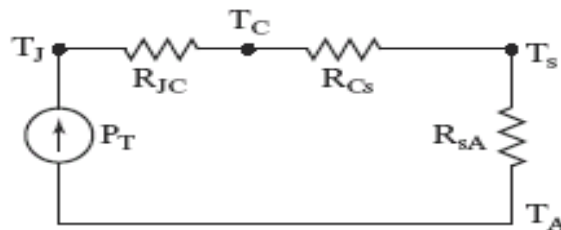


Fig.2.9: Thermal Equivalent Circuit of Transistor

5. Breakdown Voltages

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

BV_{SUS} : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

BV_{CEO} : The maximum voltage between the collector and emitter terminal with base open circuited.

BV_{CBO} : This is the collector to base break down voltage when emitter is open circuited.

6. Base Drive Control

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. t_{on} can be reduced by allowing base current peaking during turn-

on, $\left(\beta_F = \frac{I_{CS}}{I_B} \text{ forced } \beta \right)$ resulting in low forces β at the beginning. After turn on, β_F can be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. t_{off} can be reduced by reversing base current and allowing base current peaking during turn off since increasing I_{B2} decreases storage time.

A typical waveform for base current is shown.

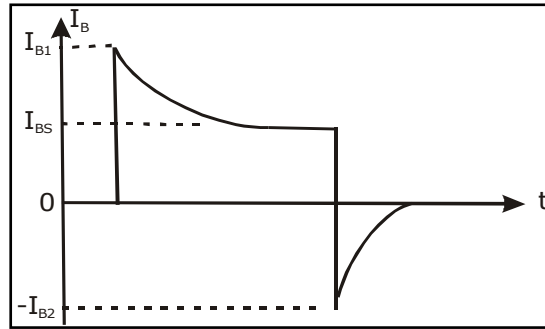


Fig.2.10: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

- Turn-on Control.
- Turn-off Control.
- Proportional Base Control.
- Antisaturation Control

Turn-On Control

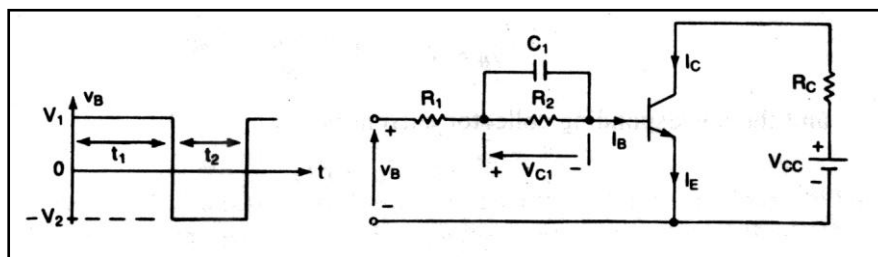


Fig. 2.11: Base current peaking during turn-on

When input voltage is turned on, the base current is limited by resistor R_1 and therefore initial value of base current is $I_{BO} = \frac{V_1 - V_{BE}}{R_1}$, $I_{BF} = \frac{V_1 - V_{BE}}{R_1 + R_2}$.

Capacitor voltage $V_C = V_1 \frac{R_2}{R_1 + R_2}$.

Therefore
$$\tau_1 = \left(\frac{R_1 R_2}{R_1 + R_2} \right) C_1$$

Once input voltage v_B becomes zero, the base-emitter junction is reverse biased and C_1 discharges through R_2 . The discharging time constant is $\tau_2 = R_2 C_1$. To allow sufficient charging and discharging time, the width of base pulse must be $t_1 \geq 5\tau_1$ and off period of the pulse must be $t_2 \geq 5\tau_2$. The maximum switching frequency is $f_s = \frac{1}{T} = \frac{1}{t_1 + t_2} = \frac{0.2}{\tau_1 + \tau_2}$.

Turn-Off Control

If the input voltage is changed to during turn-off the capacitor voltage V_c is added to V_2 as reverse voltage across the transistor. There will be base current peaking during turn off. As the capacitor C_1 discharges, the reverse voltage will be reduced to a steady state value, V_2 . If different turn-on and turn-off characteristics are required, a turn-off circuit using C_2, R_3 & R_4 may be added. The diode D_1 isolates the forward drive circuit from the reverse base drive circuit during turn off.

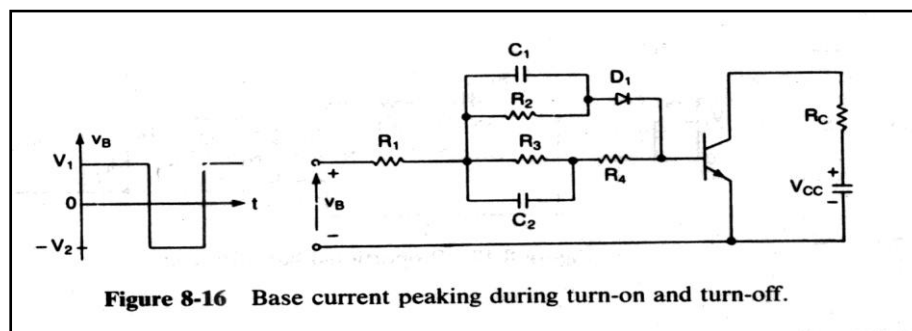


Fig: 2.12. Base current peaking during turn-on and turn-off

Proportional Base Control

This type of control has advantages over the constant drive circuit. If the collector current changes due to change in load demand, the base drive current is changed in proportion to collector current.

When switch S_1 is turned on a pulse current of short duration would flow through the base of transistor Q_1 and Q_1 is turned on into saturation. Once the collector current starts to flow, a corresponding base current is induced due to transformer action. The transistor would latch on itself and S_1 can be turned off. The turns ratio is $\frac{N_2}{N_1} = \frac{I_C}{I_B} = \beta$. For proper operation of the circuit, the magnetizing current which must be much smaller than the collector current should be as small as possible. The switch S_1 can be implemented by a small signal transistor

and additional arrangement is necessary to discharge capacitor C_1 and reset the transformer core during turn-off of the power transistor.

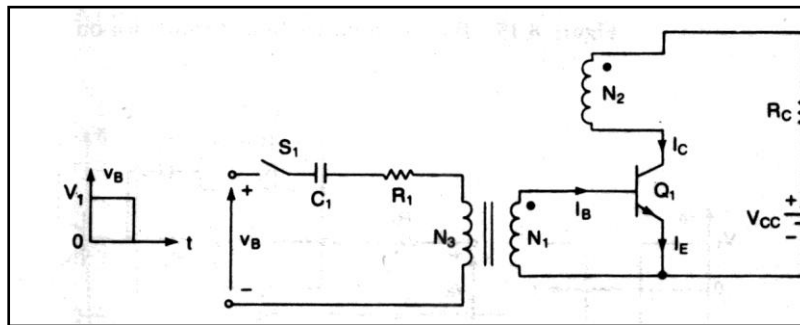


Fig.2.13: Proportional base drive circuit

Antisaturation Control

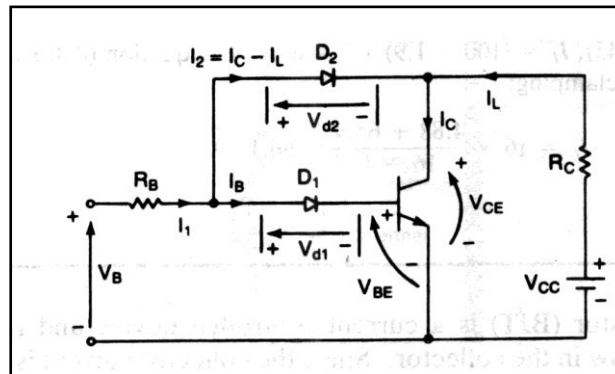


Fig.2.14: Collector Clamping Circuit

If a transistor is driven hard, the storage time which is proportional to the base current increases and the switching speed is reduced. The storage time can be reduced by operating the transistor in soft saturation rather than hard saturation. This can be accomplished by clamping CE voltage to a pre-determined level and the collector current is given by

$$I_C = \frac{V_{CC} - V_{CM}}{R_C} .$$

Where V_{CM} is the clamping voltage and $V_{CM} > V_{CE\ sat}$.

The base current which is adequate to drive the transistor hard, can be found from $I_B = I_1 = \frac{V_B - V_{D1} - V_{BE}}{R_B}$ and the corresponding collector current is $I_C = I_L = \beta I_B$.

Writing the loop equation for the input base circuit,

$$V_{ab} = V_{D1} + V_{BE}$$

Similarly $V_{ab} = V_{D_2} + V_{CE}$

Therefore $V_{CE} = V_{BE} + V_{D_1} - V_{D_2}$

For clamping $V_{D_1} > V_{D_2}$

Therefore $V_{CE} = 0.7 + \dots\dots$

This means that the CE voltage is raised above saturation level and there are no excess carriers in the base and storage time is reduced.

The load current is $I_L = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE} - V_{D_1} + V_{D_2}}{R_C}$ and the collector current

with clamping is $I_C = \beta I_B = \beta (I_1 - I_C + I_L) = \frac{\beta}{1 + \beta} I_1 + I_L$

For clamping, $V_{D_1} > V_{D_2}$ and this can be accomplished by connecting two or more diodes in place of D_1 . The load resistance R_C should satisfy the condition $\beta I_B > I_L$, $\beta I_B R_C > V_{CC} - V_{BE} - V_{D_1} + V_{D_2}$.

The clamping action thus results a reduced collector current and almost elimination of the storage time. At the same time, a fast turn-on is accomplished.

However, due to increased V_{CE} , the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.