Study of performance of Adiabatic Carry Look Ahead Adder Using Dynamic CMOS Logic

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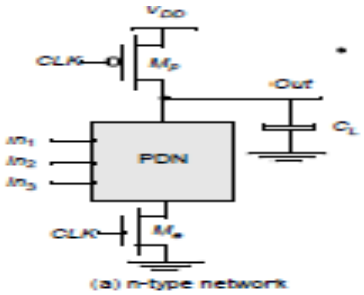
***Abstract*-Performance of adiabatic carry look ahead adder using dynamic CMOS are studied and compared with Adiabatic carry look ahead adder using Pass Transistor. adiabatic carry look ahead adder using pass transistor has higher delay and lower power consumption while adiabatic carry look ahead adder using dynamic cmos logic has lower power dissipation and higher speed. adiabatic carry look ahead adder using dynamic cmos are design using 180 nm cmos technology and compared power dissipation and delay with respect to supply voltage and frequency. simulation result show that power dissipation of carry look ahead adder using dynamic cmos has higher performance comparison adiabatic CLA using pass transistor. simulation result show that adiabatic CLA using dynamic cmos reduce the power consumption 45% and delay reduce to 70% comparison to adiabatic CLA using pass transistor.**

Introduction- For low power and higher speed circuit VLSI designer explore a new technology that dissipate low power and generate low noise. adiabatic logic using pass transistor is new approach that dissipate low power and generate low noise[2-4] but its speed is reduce comparison to other digital circuit so we proposed adiabatic logic using dynamic cmos that dissipate low power and generate low noise and show higher speed. In this paper comparative study of adiabatic CLA using pass transistor and adiabatic CLA using dynamic cmos. Dynamic CMOS logic is one of the promising circuit techniques for high speed operation [5-7]. An efficient decimal carry look ahead structure is to improve computation delay problem [8] . Static CMOS require 2N device for n fan- in while Dynamic CMOS circuit uses N+1device for n fan-in

Operation of dynamic CMOS-

There are two mode of operation.1-Precharge,2-Evaluation in the dynamic cmos design pull down network(PDN) is constructed exactly same as in complementary

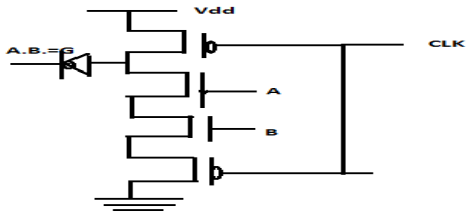


(a) n-type network

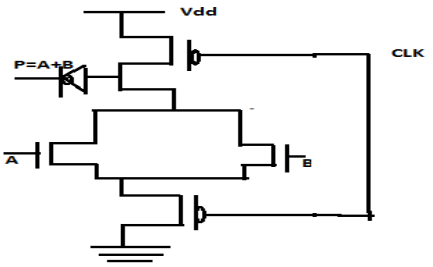
Precharge- in the dynamic CMOS PMOS transistor is precharge gate and NMOS transistor is evaluation gate .when clock is zero(CLK=0) output node is precharge to V_{dd} by the PMOS transistor Mp while evaluate NMOS transistor is off so the pull-down path is disabled. evaluation transistor (NMOS) eliminates any static power dissipation that would be consumed by the precharge period.

Evaluation – when CLK=1 precharge transistor (Mp) is off and evaluation transistor is on during this time output is discharg*e* based on input value. if the input are such that PDN conduct then a low resistance path exist between output and GND and output is discharged to GND. If the PDN is off then precharge value is stored on the output capacitance C_L. Once output node is discharge then it cannot be charged again till the next precharge operation.Output canbe high impedance state during the evaluation period if the pull down network is off

Design of Adiabatic CLA using dynamic CMOS- here we design the 4 bit adiabatic CLA using Dynamic CMOS .AND gate and OR gate using Dynamic CMOS logic .In the Dynamic CMOS logic design only higher mobility of transistor is used so the Dynamic CMOS circuit performance increase and due to absence of PMOS input capacitance also low .AND gate and OR gate circuit is given below .



AND GATE USING DYNAMIC CMOS

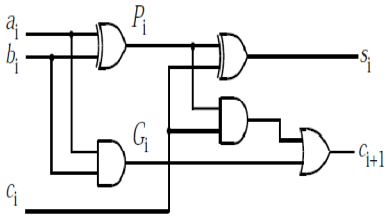


OR GATE USING DYNAMIC CMS

Carry generation and propagation- Carry Look Ahead Adder solve the carry delay problem by calculating the carry signal in advance. It is based on the carry signal will be generated in two cases(1) when both bit a_i and b_i are 1 (2) when one of the two bit is 1 and carry-in is 1.

$C_i=a_i + b_i + (a_i \oplus b_i)C_i$

$S_i= (a_i \oplus b_i) \oplus C_i$ these two signal can be written in two new signal P_i and G_i



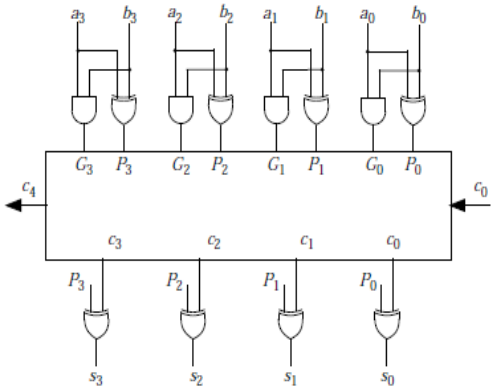
full adder $C_{i+1} = G_i + P_i C_i$

$S_i = P_i \oplus C_i$ where $G_i = a_i.b_i$ and $P_i = a_i \oplus b_i$ where G_i and P_i are carry generate and carry propagate term respectively. Carry generate and propagate term only depend on the input bit and thus will be valid after one and two gate respectively. If one use above expression to calculate the carry signal one does not need to wait for the carry to ripple through all the previous stage to find its proper value. Let's apply this to a 4 bit adder to make it clear

$C_1 = G_0 + P_o C_0$

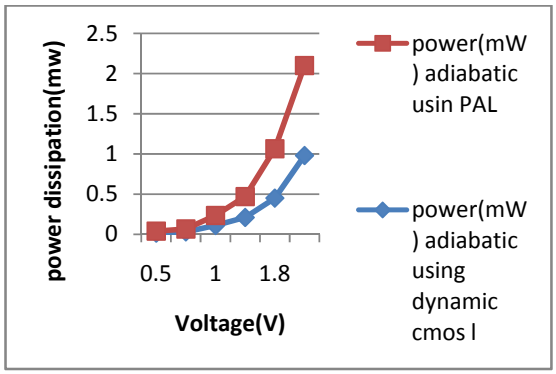
$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

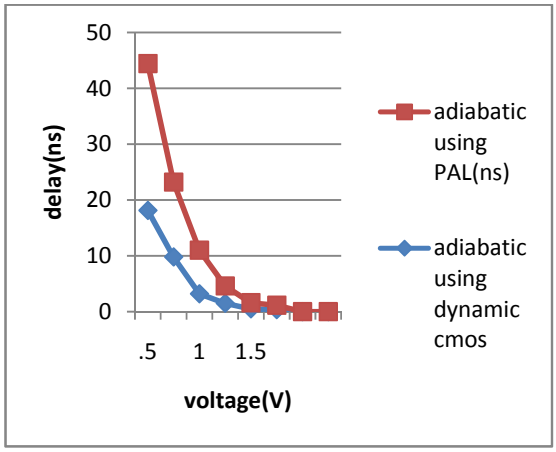
$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$



$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

Simulation Result-





From the graph we see that power consumption and delay both decrease when supply voltage is increase in the adiabatic CLA using dynamic CMOS logic while in the adiabatic CLA using PAL power consumption decrease but delay is increase. So from the simulation result it is clear that adiabatic circuit using dynamic CMOS logic has higher speed and lower power consumption**.**

Result-based on HSPICE simulation 180 nm CMOS technology show result 4- bit adiabatic CLA using dynamic CMOS exhibit energy saving 45% and decrease in delay 34% comparison to adiabatic CLA using pass transistor. But comparison to pal dynamic CLA is costly**.**

Conclusion- form the graph we see that both CLA using PAL and dynamic logic show the power reduction but in PAL CLA it show higher delay comparison to dynamic cmos logic .

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