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Simulations of Carbon Nanotube Field Effect Transistors

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Abstract

As the scaling of Si MOSFET approaches towards its limiting value, new alternatives are coming up to overcome these limitations. In this paper first we have reviewed carbon nanotube field effect transistor (CNTFET) and types of CNTFET. We have then studied the effect of channel length and chirality on the drain current for planer CNTFET. The I_d~V_d curves for planer CNTFETs having different channel lengths and diameters are plotted. For the same, I_d~V_d curves for different applied gate voltages are also plotted. We have then discussed the effect of diameter on the characteristic curves for a cylindrical CNTFET. Finally a brief comparison between the performance of Si-MOSFET and CNTFET is given.

Introduction

Silicon-based technology has experienced phenomenal growth in the last few decades. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. Though this trend still continues, bulk MOSFET will soon reach its limiting size. For this reason, the semiconductor industry is looking for different materials and devices to integrate with the current silicon-based technology and in the long run, possibly replace it. The carbon nanotube field effect transistor is one among the most promising alternatives due to its superior electrical properties.

This paper reviews different types of CNTFET which are one of the most promising devices to replace Si MOSFET in near future and also gives an insight for some basic characteristics of CNTFET. It is organized as follows. CNTFET and types of CNTFET are discussed in section 2. Section 3 comprises of some simulation results for planar CNTFET. Cylindrical CNTFET and the effect of diameter for cylindrical CNTFET are discussed in section 4. A brief comparison between Si-MOSFET and CNTFET is given in section 5 and we conclude the paper in section 6.

Carbon nanotube field effect transistor (CNTFET)

Single walled carbon nanotubes (SWCNTs) have huge potential for applications in electronics because of both their metallic and semiconducting properties and their ability to carry high current. CNTs can carry current density of the order 10 μA/nm^2, while standard metal wires have a current carrying capability of the order 10 nA/nm^2.

Semiconducting CNTs have been used to fabricate CNTFETs, which show promise due to their superior electrical characteristics over silicon based MOSFETs. Since the electron mean free path in SWCNTs can exceed 1 micrometer, long channel CNTFETs exhibit near-ballistic transport characteristics, resulting in high-speed devices. The first CNTFET was fabricated in 1998[1]. In the same year R. Martel et.al.[2] fabricated field-effect transistors based on individual single- and multi-wall carbon nanotubes and analyzed their performance. The broad classifications of CNTFET are discussed below.

Geometry dependent CNTFET

a. Back-gate CNTFET

The first back gate CNTFET was proposed by Tans et.al. [1]. In this structure a single SWCNT was used to bridge two noble metal electrodes prefabricated by lithography on an oxidized silicon wafer. Here the SWCNT plays the role of channel and the metal electrodes act as source and drain. The heavily doped silicon wafer itself behaves as the back gate. These CNTFETs behaved as p-type FETs with an I (on)/I (off) ratio~10^5. The schematic diagram of back-gate CNTFET is shown in figure-1. This suffers from some of the limitations like high parasitic contact resistance (≥1Mohm), low drive currents (a few nanoamperes), and low transconductance $g_m \approx$ 1nS [3]. To reduce these limitations the next generation CNTFET developed which is known as top gate CNTFET.

b. Top gate CNTFET

To get better performance Wind et al. proposed the first top gate CNTFET in 2003[4]. Figure-2 shows the schematic diagram of a top-gated CNTFET with Ti source, drain, and gate electrodes. A 15-nm SiO_2 film was used as the gate oxide. Here gate is placed over the CNT. The advantage of top gated CNTFET over back gated CNTFET is summarized in table-I. These data are taken from [3].

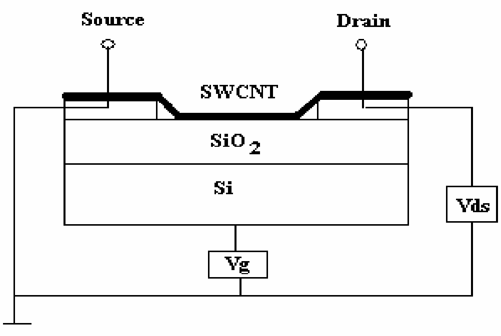

Figure 1: A back-gate CNTFET.

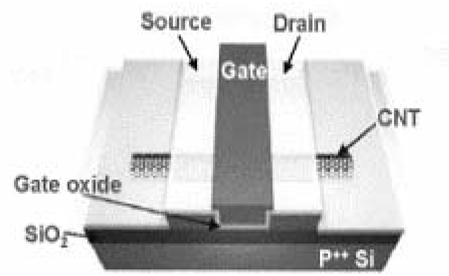

Figure 2: A top-gate CNTFET [3].

Table I: Comparison between Back gate CNTFET and Top gate CNTFET.

Parameters	Back gate CNTFET	Top gate CNTFET
Threshold voltage	-12V	-0.5V
Drain current	Of the order of nanoampere	Of the order of microampere
Transconductance	1nS	3.3μS
I(on)/I(off)	10^5	10^6

Electrodes dependent CNTFET
Based on the type of electrodes used CNTFET is classified into three categories.

(a) Schottky-barrier (SB) CNTFET (b) Partially gated (PG) CNTFET and (c) doped-S/D CNTFET. [5, 6]

a. Schottky-barrier (SB) CNTFET
As shown in figure-3(a), in this type of CNTFET an intrinsic CNT is used in the channel region. This is connected to metal Source/Drain and forms Schottky barriers at the junctions. Carbon nanotube transistors operate as unconventional Schottky barrier transistors in which transistor action occurs primarily by varying the contact resistance rather than the channel conductance. These types of FET require careful alignment of the Schottky barrier and gate electrode which leads to manufacturing challenge. Also the presence of Schottky barrier lowers the on-current. These are explored further in references [7,8,9,10].

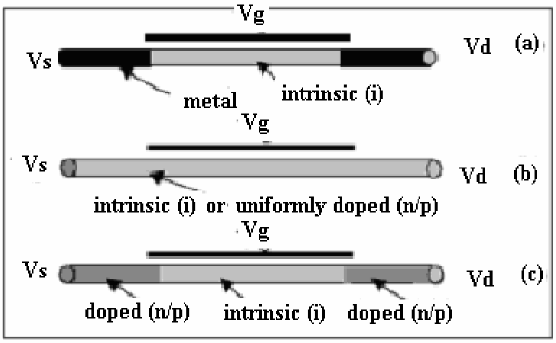

Figure 3: Different types of CNTFET: (a) Schottky-barrier (SB) CNTFET, (b) partially gated (PG) CNTFET (c) doped-S/D CNTFET [5].

b. Partially gated (PG) CNTFET

PG-CNTFET, shown in fig.3 (b), is a depletion mode CNTFET in which the nanotube is uniformly doped or uniformly intrinsic with ohmic contacts at their ends. PG-CNTFETs can be of n-type or p-type when respectively n-doped or p-doped. In these devices the gate locally depletes the carriers in the nanotube and turns off the p-type (n-type) device with an efficiently positive (negative) threshold voltage that approaches the theoretical limit for room-temperature operation. The on-current of such devices is given as I_D (on) $=q\rho v_t$ where ρ is the carrier density per unit length and v_t is the uni-directional thermal velocity [5-6].

c. Doped- source or drain (S/D) CNTFET

Doped-S/D CNTFETs presented in fig.3(c) are composed of three regions. The region below the gate is intrinsic in nature and the two ungated regions are doped with either p-type or n-type. The ON-current is limited by the amount of charges that can be induced in the channel by the gate and not by the doping in the source. They operate in a pure p- or n-type enhancement-mode or in a depletion-mode, based on the principle of barrier height modulation when applying a gate potential.

Out of these three, doped S/D CNTFETs are promising because (1) they show unipolar characteristics unlike SB-CNTFETs; (2) the absence of SB reduces the OFF leakage current; (3) they are more scalable compared to their SB counterparts; (4) in ON-state, the source-to-channel junction has a significantly higher ON current.

Depending on the doping profile doped S/D CNTFETs can again be classified into two groups.

(a) Conventional CNTFET (C-CNTFET): This comprise of CNTFETs with p/i/p or n/i/n doping scheme that is both S/D are doped with either p-type or n-type material.

(b) Tunneling CNTFET (T-CNTFET): CNTFETs with n/i/p doping scheme (source and drain are oppositely doped) comes under this group [11].

All the CNTFETs discussed till are of planer structure. Besides these planar structures one more structure is also developed which is known as vertical CNTFET (V-CNTFET) or coaxially gated CNTFET. This consists of a SWCNT with a coaxial gate. The advantage of V-CNTFET is that vertical growth in CNT is easier and aligned than horizontal growth.

Besides all these configurations double gate CNTFET and Nanotube on insulator CNTFET (NOI CNTFET) similar to silicon on insulator (SOI) technology are also reported. Now-days some modified structures are also developed by different reseachers to yield better performance. We have given a brief discussion of these structures below.

Ji-Yong Park has developed a CNTFET with a CNT gate electrode of width nearly 3nm and compared its response to one with a back gate electrode [12]. In order to prepare a CNT gate electrode, devices with more than one CNT between source and drain electrodes are identified by scanning electron microscopy or AFM imaging to utilize one of the CNTs as a gate electrode. Then this local CNT gate is connected to the voltage source either by e-beam lithography or by using a gold coated AFM tip as an interconnect to the CNT gate. Due to the much smaller gate width compared to the whole device length, it is decoupled from the contact area, which is represented by sharp turn-off and almost constant turn-on current. This CNTFET is shown to have higher transconductance and smaller subthreshold slope with the CNT gate compared to values with the global back gate.

A new structure for carbon nanotube field effect transistors (CNTFETs) has been proposed recently and its current-voltage characteristic has been simulated by Zoheir Kordrostami et.al.[13]. One end of the carbon nanotube which forms the source is put in contact with the metal intrinsically and the other end of the CNT which forms the drain is doped with potassium and then contacted to the metal. This kind of CNTFET is known as Schottky-Ohmic CNTFET (SO-CNTFET). Its current-voltage characteristic is unipolar. The off-current of the SO-CNTFET has a lower magnitude than conventional SB-CNTFETs and occurs in zero gate voltage. This is because in the SO-CNTFET against the SB-CNTFET case, in all the bias voltages the majority carriers are electrons and the current originates from the tunneling of the electrons from the Schottky barrier at the source.

Simulation results for planer CNTFET

We have simulated different CNTFETs having planer structure to see how the characteristic curves depend on different tube parameters like the length of the tube and the chirality. For this simulation we have used the nanohub simulators [14-16]. First we simulated a CNTFET where a (10,0) cnt is used as channel. For this simulation we have kept all other parameters fixed and changed the channel length as well as the top gate length proportionally. Secondly we have changed the diameter, by changing the chirality, and kept the channel length constant. If (n,m) is the chirality of a CNT, the diameter of the CNT is given as: $d = a\,(n^2+m^2+nm)^{1/2}/\pi$ where a is the length of the graphene basis vector.

The structure used for simulation is shown in figure-4. Figure-5 shows the I_d~V_d curves for different CNTFETs. These are plotted for three cases: (i) (10,0) CNT with channel length 10nm and gate length 8nm, (ii) (10,0) CNT with channel length 15nm and gate length 12nm and (iii) (13,0) CNT with channel length 10nm and gate length 8nm. Comparing the first two it is clear that keeping the diameter of CNT fixed if we are changing the length of CNT i.e. the channel length of a CNTFET then we will get higher saturation current for smaller channel length. Again comparing the curves for first and third set which are for different chiralities, the saturation drain current is higher for a CNTFET consisting of smaller diameter keeping the length constant.

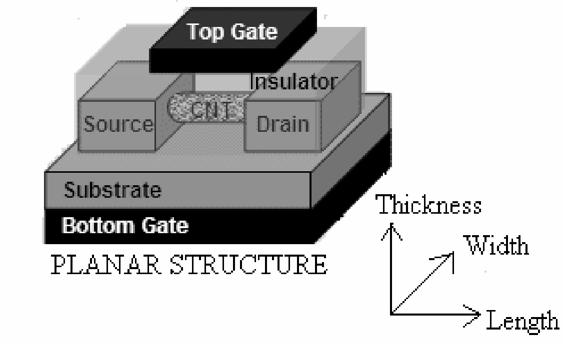

Figure 4: Structure considered for simulation.

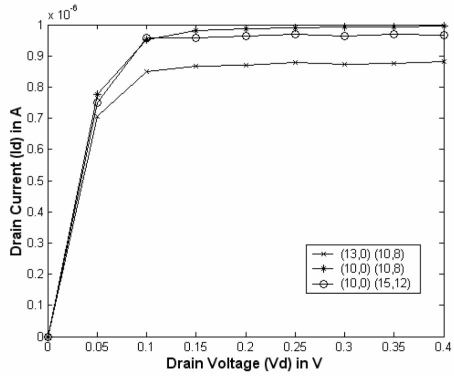

Figure 5: I_d~V_d curves for different CNTFETs.

For a planer CNTFET, we have also plotted the output characteristic curves (I_d~V_d curves) for different applied gate voltage which are shown in figure-6. For this we have considered a planar CNTFET with a (10,0) CNT as the channel and channel length 10nm. The range of drain voltage considered is 0V to 0.4V and the plots are for gate voltages 0.1V, 0.2V, 0.3V and 0.4V. The drain current is almost zero for first two plots which are for gate voltages 0.1V and 0.2V as these gate voltages are below the threshold voltage. Again the current increases with applied gate voltage.

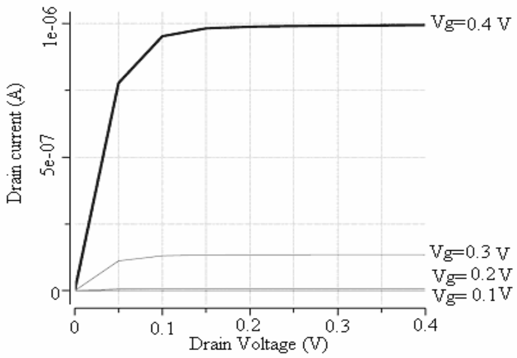

Figure 6: I_d~V_d curves for different applied gate voltages.

Simulation results for co-axial (cylindrical) CNTFET

The channel region of the structure considered for simulation of cylindrical CNTFET is shown in figure-7 below.

In cylindrical CNTFET, a CNT is used as the channel which is surrounded by an oxide layer which is finally surrounded by a metal contact. This metal contact serves as the gate terminal. This simulation is done by using the nanohub simulator [17-18]. In this simulation we have taken the threshold voltage V_t=0.2V, and diameter of CNT was varied from 2nm to 5nm. SiO_2 (k=3.9) is the gate insulator with thickness t = 1.5nm. The results of the simulation are plotted in figure-8.

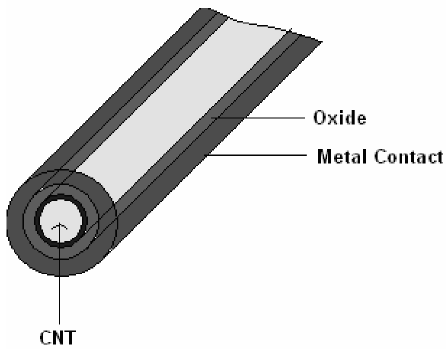

Figure 7: structure for cylindrical CNTFET.

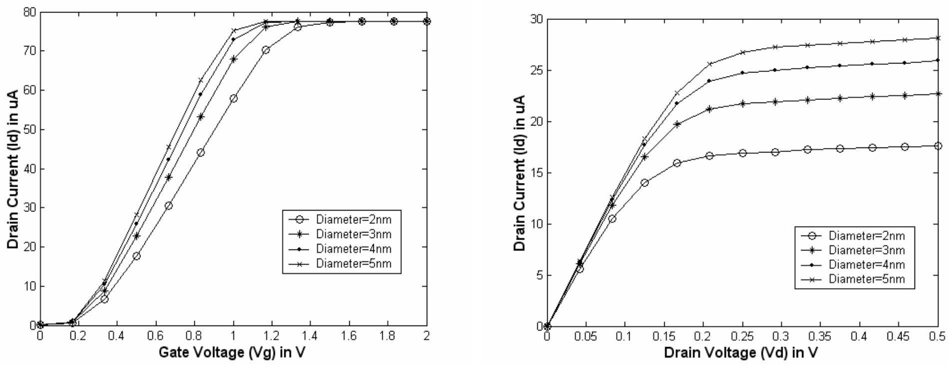

Figure 8: (a) Gate voltage (V_g) ~ Drain current (I_d) (b) Drain voltage (V_d) ~ Drain current (I_d) plots for cylindrical CNTFET

Transfer characteristics for different diameters of CNT are plotted in figure-8(a), which shows that the effect of diameter is more significant in lower region of gate bias. The switching speed is more for larger diameter i.e. as the diameter increases the device approaches saturation faster. Figure-8(b) shows the output characteristics for different diameters of CNT used in the channel region. From the figure it is clear that the drain current is more for higher values of diameter and the difference decreases as we go for higher values of diameter.

Comparison between CNTFET and MOSFET

In this section we have given a brief comparison between the performance of CNTFET and MOSFET.

(i) In case of Si-MOSFET switching occurs by altering the channel resistivity but for CNTFET switching occurs by the modulation of contact resistance.
(ii) CNTFET is capable of delivering three to four times higher drive currents than the Si MOSFETs at an overdrive of 1 V.

(iii) CNTFET has about four times higher transconductance in comparison to MOSFET.

(iv) The average carrier velocity in CNTFET is almost double that in MOSFET.

The on-current performance advantage of the CNTFET is either due to the high gate capacitance or due to the improved channel transport. The improved channel velocity for the CNTFET is due to the increased mobility and band structure of CNTFET.

Conclusion

This paper basically gives an insight into the existing types of CNTFET. This also discuses some characteristic curves for both planar CNTFET and coaxial CNTFET. The length, chirality and diameter dependence of the characteristic curves are also discussed. Finally we have compared the performance advantages of CNTFET over Si MOSFET.

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