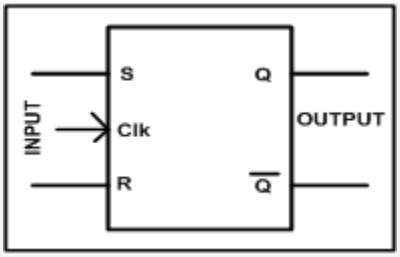
SR Flip Flop Design with NOR and NAND Logic Gates

The SR Flip Flop is one of the fundamental parts of the sequential circuit. SR is a digital circuit and binary data of a single bit is being stored by it. RS Flip Flop has two stable states in which it can store data i.e. either binary zero or binary one. The Flip Flop has remained in the state until we changed the state i.e. if the RS is set to binary one then it will remain in that state until we changed the state or the power is off. It implies that the flip flop memorize the state in which it was earlier set and remember the date that given to it. SR flip flop is designed here with the use of NOR gate by us.

Description:

SR Flip Flop also known as SR latch is the most vital as well as broadly used Flip Flop. It is further more acknowledged as SET-RESET Flip Flop. Below the symbolic representation of the SR Flip Flop is shown:



Symbolic Representation of SR Flip Flop

R and S are the two input terminals in the SR Flip Flop. The Flip Flop is set by the input terminal S while Flip Flop is reset by the input terminal R. Q and Q^{-} are the two output terminals in the Flip Flop and both are complimentary of each other. Flip Flop is said to be in the set condition when it is stored 1and if 0 is stored, Flip Flop is reset.

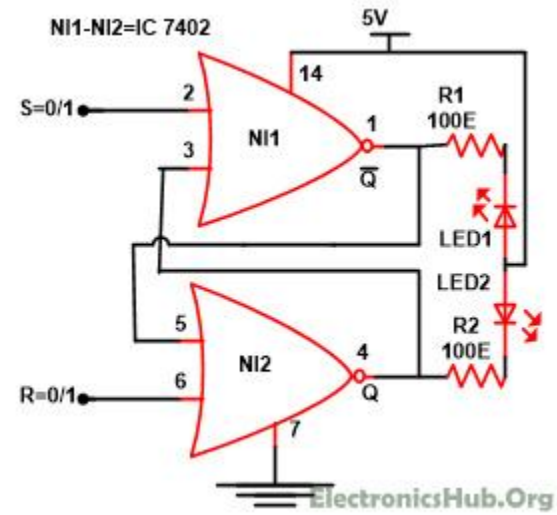
In the below, table states of the Flip Flop is shown.

Flip Flop	Output	
State	Q	$\bar{Q}$
SET	1	0
RESET	0	1

SR Flip Flop States Representation

Design of SR Flip Flop with NOR Gate:

Below we have shown that how SR Flip Flop can be designed using NOR gate. In the circuit diagram, there are two input terminals S and R. Understanding of the truth table of NOR gate is important before knowing the working of the circuit. In the NOR gate, if the input at both the terminals is low i.e. 0 then only we get the output high i.e. 1. If any of the input terminals or both of the inputs are in high state i.e. 1, then output will be low i.e. 0.



SR Flip Flop with NOR Gate –ElectronicsHub.Org

Functioning of SR Flip Flop is very easy.

Now imagine that at the input terminal of Flip Flop, we applied S=0 and R=0, at these condition states of Flip Flop will not change and it will stay on its present condition.

Assume that S=0 and R=1 then in that condition the output at upper NOR gate will be low. Hence the input at both the lower gate is in low state so the output we got will be high. This in turn provide 1 at the R input and as a result of it Flip Flop reaches at stable condition where Q=0 with $\overline{Q}$=1. I this mode the Flip Flop will reset by its own and LED 1 will start glowing this time.

Now assume that S=1 and R is set to 0, at this condition the lower NOR gate output switch to low and turn the input of the upper gate switch to low and output got will be high. Hence at the moment we can articulate that at S=1 the Flip Flop sets of input and Flip Flop move to a stable condition where Q=1 and$\overline{Q}$=0. In this condition Flip Flop will set by its own and LED 2 will glow this time.

Now suppose input at both S and R is 1. In this condition both the output of NOR gate goes to low and as a result of its output at Q and $\overline{Q}$ is 0 and this will contradict the definition of the Flip Flop which defines that the outputs are complimentary of each other. So this condition is practically not possible and both LED will start glowing.

The following table summarizes the above explained working condition of the NOR Flip Flop gate.

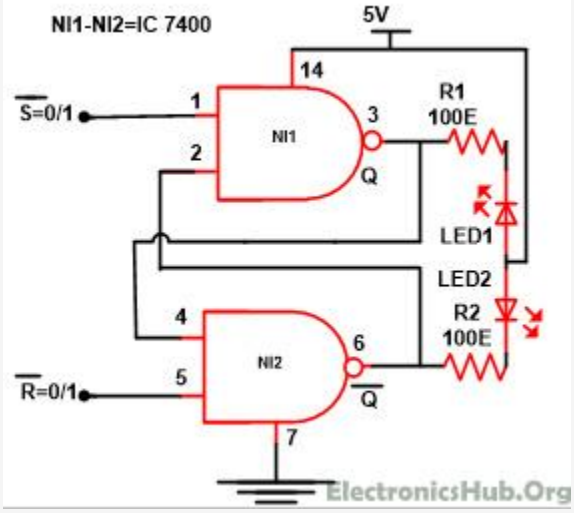
Working Condition of NOR Flip Flop Gate:

S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

NOR Flip Flop Gate Working Conditions

SR Flip Flop Design with NAND Gate:

In the circuit diagram, there are two inputs named R and S. The truth table of the NAND gate must be understood by one before getting into the working of the circuit. If both the inputs are high ie 1 than in that case only the output is low, otherwise if any of the input is high or if both the input is high the output will be high.



SR Flip Flop with NAND Gate –ElectronicsHub.Org

Functioning of SR Flip Flop is very easy.

Imagine that at the input of SR Flip Flop we have given S^{-}=1 and R^{-}=1, the state of the input will not change and it will stay in its present state.

The upper NAND gate output will become high when S^{-}=0 and R^{-}=1. Hence both the lower NAND gate input goes to high and low output will receive. Hence at the R terminal we will get 1 and Flip Flop reaches to a stable state and in these conditions Q=1and Q^{-}=0. Flip Flop will set by its own and LED2 light will glow at this time.

Lower NAND gate output will move to high at S^{-}=1 and R^{-}=0,which in turn the upper NAND gate move to high and low output will get. Therefore at this time we can state that a 1 at S^{-}input sets the Flip Flop and in turn of it Flip Flop moves to a stable condition where Q=0 and Q^{-}=1. In this condition Flip Flop will set by its own and LED 1 will start glowing.

Now assume both $S^{-}$and $R^{-}$is 0 at this instance both the NAND gates output become's high, output at Q=1 and Q^{-}=1 and this contradicts the definition of the Flip Flop which implies that the output of Flip Flop are complimentary of each other. So the situation is practically not achievable and both LED will not glow.

The table below summarizes above explained working of SR Flip Flop designed with the help of a NAND gate.

Working Condition of NAND Flip Flop Gate:

$\overline{S}$	$\overline{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

Working of SR Flip Flop with NAND Gate

Source: http://www.electronicshub.org/sr-flip-flop-design-with-nor-and-nand-logic-gates/