**D0 - D7** These are the data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines.

**CS (Chip Select Input).** If this line is a logical 0, the microprocessor can read and write to the 8255.

**RD (Read Input)** Whenever this input line is a logical 0 and the RD input is a logical 0, the 8255 data outputs are enabled onto the system data bus.
**WR (Write Input)** Whenever this input line is a logical 0 and the CS input is a logical 0, data is written to the 8255 from the system data bus.

**A0 - A1 (Address Inputs)** The logical combination of these two input lines determines which internal register of the 8255 data is written to or read from.

**RESET** The 8255 is placed into its reset state if this input line is a logical 1. All peripheral ports are set to the input mode.

**PA0 - PA7, PB0 - PB7, PC0 - PC7** These signal lines are used as 8-bit I/O ports. They can be connected to peripheral devices. The 8255 has three 8 bit I/O ports and each one can be connected to the physical lines of an external device. These lines are labeled PA0-PA7, PB0-PB7, and PC0-PC7. The groups of the signals are divided into three different I/O ports labeled port A (PA), port B (PB), and port C (PC).

### 4.2.3 Operational Modes of 8255

There are two main operational modes of 8255:

1. Input/output mode  
2. Bit set/reset mode

#### Input/Output Mode

There are three types of the input/output mode. They are as follows:

**Mode 0**

In this mode, the ports can be used for simple input/output operations without handshaking. If both port A and B are initialized in mode 0, the two halves of port C can be either used together as an additional 8-bit port, or they can be used as individual 4-bit ports. Since the two halves of port C are independent, they may be used such that one-half is initialized as an input port while the other half is initialized as an output port. The input output features in mode 0 are as follows:

1. O/p are latched.  
2. I/p are buffered not latched.  
3. Port do not have handshake or interrupt capability.

**Mode 1**

When we wish to use port A or port B for handshake (strobed) input or output operation, we initialise that port in mode 1 (port A and port B can be initialised to operate in different modes, ie, for eg, port A can operate in mode 0 and port B in mode 1). Some of the pins of port C function as handshake lines. For port B in this mode (irrespective of whether is acting as an input port or output port), PC0, PC1 and PC2 pins function as handshake lines. If port A is initialised as mode 1 input port, then, PC3, PC4 and PC5 function as handshake signals. Pins PC6 and PC7 are available for use as input/output lines. The mode 1 which supports handshaking has following features:

1. Two ports i.e. port A and B can be use as 8-bit i/o port.  
2. Each port uses three lines of port c as handshake signal and remaining two signals can be function as i/o port.  
3. interrupt logic is supported.  
4. Input and Output data are latched.

**Mode 2**
Only group A can be initialised in this mode. Port A can be used for bidirectional handshake data transfer. This means that data can be input or output on the same eight lines (PA0 - PA7). Pins PC3 - PC7 are used as handshake lines for port A. The remaining pins of port C (PC0 - PC2) can be used as input/output lines if group B is initialised in mode 0. In this mode, the 8255 may be used to extend the system bus to a slave microprocessor or to transfer data bytes to and from a floppy disk controller.

**Bit Set/Reset (BSR) mode**

In this mode only port b can be used (as an output port). Each line of port C (PC0 - PC7) can be set/reset by suitably loading the command word register. No effect occurs in input-output mode. The individual bits of port c can be set or reset by sending the signal OUT instruction to the control register.

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