PARALLEL COMMUNICATION INTERFACE AND FUNCTIONAL BLOCK DIAGRAM

The **Intel 8255** (or **i8255**) Programmable Peripheral Interface chip is a peripheral chip originally developed for the Intel 8085 microprocessor, and as such is a member of a large array of such chips, known as the **MCS-85 Family**.This chip was later also used with the Intel 8086 and its descendants. It was later made (cloned) by many other manufacturers. It is made in DIP 40 and PLCC 44 pins encapsulated versions.

This chip is used to give the CPU access to programmable parallel I/O, and is similar to other such chips like the Motorola 6520 PIA (Peripheral Interface Adapter) the MOS Technology 6522 (Versatile Interface Adapter) and the MOS Technology CIA (Complex Interface Adapter) all developed for the 6502 family. Other such chips are the 2655 Programmable Peripheral Interface from the Signetics 2650 family of microprocessors, the 6820 PIO (Peripheral Input/Output) from the Motorola 6800 family, the Western Design Center WDC 65C21, an enhanced 6520, and many others.The 8255 is widely used not only in many microcomputer/microcontroller systems especially Z-80 based, home computers such as SV-328 and all MSX, but also in the system board of the best known original IBM-PC, PC/XT, PC/jr, etc. and clones.However, most often the functionality the 8255 offered is now not implemented with the 8255 chip itself anymore, but is embedded in a larger VLSI chip as a sub function. The 8255 chip itself is still made, and is sometimes used together with a micro controller to expand its I/O capabilities.

4.2.1Functional Block diagram:

The 8255 has 24 input/output pins in all. These are divided into three 8-bit ports. Port A and port B can be used as 8-bit input/output ports. Port C can be used as an 8-bit input/output port or as two 4-bit input/ouput ports or to produce handshake signals for ports A and B.

The three ports are further grouped as follows:

1) Group A consisting of port A and upper part of port C.
2) Group B consisting of port B and lower part of port C.

Eight data lines (D0 - D7) are available (with an 8-bit data buffer) to read/write data into the ports or control register under the status of the "$\overline{\text{RD}}$" (pin 5) and $\overline{\text{WR}}$" (pin 36), which are active low signals for read and write operations respectively. The address lines A1 and A0 allow to successively access any one of the ports or the control register as listed below:

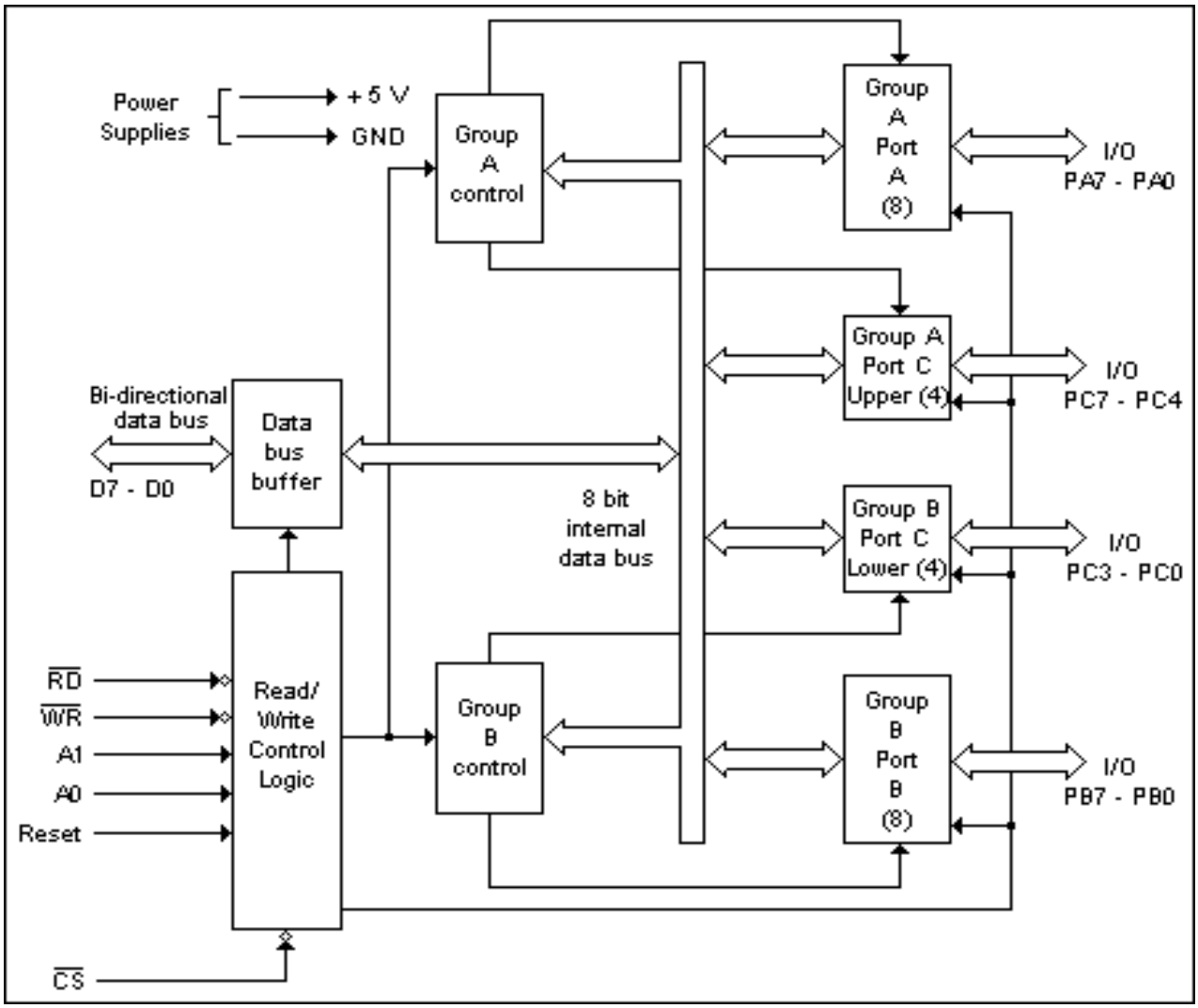

FIGURE 1

A1	A0	Function
0	0	port A
0	1	port B
1	0	port C
1	1	control register

The control signal "'−*CS"* ***(pin 6) is used to enable the 8255 chip. It is an active low signal, ie, when*** **−CS = '0**, the 8255 is enabled. The **RESET** input (pin 35) is connected to a system (like 8085, 8086, etc.) reset line so that when the system is reset, all the ports are initialised as input lines. This is done to prevent 8255 and/or any peripheral connected to it, from being destroyed due to mismatch of ports. This is explained as follows. Suppose an input device is connected to 8255 at port A. If from the previous operation, port A is initialised as an output port and if 8255 is not reset before using the current configuration, then there is a possibility of damage of either

the input device connected or 8255 or both since both 8255 and the device connected will be sending out data.

The control register or the control logic or the command word register is an 8-bit register used to select the modes of operation and input/output designation of the ports.

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