OVERVIEW OF VLSI FABRICATION FACILITY

Nano fabrication facilities are inevitable for the mass production of integrated circuits. Manufacturing nano range of patterns requires complex process steps to be followed in ultra clean environment. Huge amount of capital in terms of both money and intellectual are necessary to setup a manufacturing facility. As feature size reduces from one node to another smaller node, the installed fabrication equipments may not be compatible to the new node. Thus life time of the fabrication plant is limited by the life time of the node technology. To reduce the cost and to improve the overall throughput in a lesser time, careful design of fabrication facility is important. As and when technology advances the design should provide maximum opportunity to expand to a newer node with less reinvestment.

CMOS process technology

There is not much change in the basic technology used for semiconductor device manufacturing process for last 3 decades. Significant improvements have been made to different processing steps like depositing, etching, diffusing and patterning. Present day technology uses wafers having thickness upto 750 micron. Top surface layer thickness has reduced to 1 micron.

In CMOS technology both nMOS and pMOS transistors are fabricated side by side on the same substrate. Multiple levels of metal and planarization is used in this process. Chip crossection is dominated by interconnection layer. CMOS process technology has advantages of low DC power consumption, high performance and flexible design options. The main technologies to do the fabrication of IC are **p-well, n-well, twin tub and Silicon On Insulator (SOI) CMOS process**.

In ***p-well process*** the substrate is N-type. N channel device is formed into the p-well. The p channel device is directly constructed on the substrate itself. For ***n-well*** it is reverse. In***twin tub or twin well*** process both n-well and p-well are fabricated on single N-type substrate. It is possible to tune independently threshold voltage, body effect and the channel transconductance of both P and N type transistors using this process. With n+ or p+ as starting material , lightly doped epitaxial layer is formed on this layer n-well and p-well are formed. Unbalanced drain parasitics are observed in p and n well CMOS process. Twin tub process avoids this problem.

Silicon On Insulator (SOI) process technology makes it possible to fabricate completely isolated pMOS and nMOS transitors side by side. Advantages of SOI process over other CMOS

technologies are avoidance of latch up problem, low parasitic capacitances, higher integration density and higher speed.

Process plan

The overall view of the complete CMOS process flow for the fabrication of integrated circuit is briefly explained below.

- **Crystal growth and wafer slicing process:**

Step1: obtaining the sand: sand with very good form of clean silicon is used to grow the wafer.

Step2: preparing the molten silicon bath: the sand(SiO_2) is heated just above its melting point temperature of 1600ºC.

Step3: making the ingot: a seed containing desired crystal orientation is placed onto the molten sand bath. This crystal is slowly pulled out(1mm/minute). Czochralski(CZ) method is used for this process. The resultant pure silicon is called an ingot.

Step 4: preparing the wafers: with a diamond saw ingot is sliced into very thin wafers.

- **Thickness sorting:** Sliced wafers are sorted on an automated basis into bathes of uniform thickness.
- **Lapping and etching:** Cracked or damaged surface of the silicon wafer due to slicing is removed by lapping. Crystal damages are removed by etching process.
- **Thickness sorting and flatness checking:** Once again wafers are sorted acording to their thickness.
- **Polishing process:** This process can be either mechanical or chemical or both. Here uneven surface left by lapping and etching processes are smoothened.

Final dimensions and electrical properties qualification: the wafers undergo final test to satisfy customer requirement of flatness , thickness, resistivity and type.

Fabrication:

The prepared wafers are exposed to multiple levels of photolithography process. Each step is repeated for each mask. Mask defines the different layers of the integrated circuit pattern which are designed using CAD tools.

First ixide(SiO_2) layer is formed on the wafer.

- **Photolithography:** Photoresist coating is applied on the surface of wafer. Wafer is aligned with mask and light source. In the transparent areas of mask light passes through and exposes the photoresist.
- **Direct wafer stepping:** In this method mask is kept away from the wafer. With the help of series of optics image is placed on to the wafer. This technique allows larger mask size than the final pattern. Exposed regions of photoresist becomes hard.
- **Etching the wafer surface:** This process removes unwanted material from the wafer. There are two main methods of etching: ***wet etching*** and ***dry etching*****.**
- **Wet etching:** Chemicals are used for wet etching. Number of wafers are dipped in concentrated acid and exposed areas of wafers are etched away.
- **Dry etching:** Gas is used instead of chemical etchants.
- **Plasma etching:** An intense electric field is applied to generate the plasma state of gaseous matter. Gases used are very reactive in plasma state. This provides effective etching of exposed surface.
- ***Reactive ion etching*** and ***ion milling*** are the other two techniques used for etching.

Implant/masking: diffusion and ion implant:

- **Diffusion:** First photoresist is coated and patterning is done using photolithography process. Then wafer is kept in a furnace with a flow of gas running over the wafers. Dopants are slowly diffused.
- **Ion implantation:** Here desired dopant ions are shooted (or implanted) into the wafer. This process can handle single wafer at a time while diffusion chamber can handle many wafers at a time.
- **Drive in:** Wafers are heated so that implanted(or diffused) ions are go deeper into the wafer.
- **Annealing: C**rystal lattice structure of the wafer is disturbed by the diffusion or ion implantation. To repair this wafer is heated so that crystal structure is repeated itself.

The circuit elements are fabricated with different mask operations. Some of the final masks define interconnections.

A passivation layer is coated to protect the entire wafer from the contamination during assembly. Passivation material is etched from the bonding pads using final mask and passivation etch. Then all ICs are tested for its functionalty and non functional ICs are marked. A diamond saw is used to cut the wafer into indivisual chips.

- **Die attach/wire bond:** Die is mounted on to the lead frame. A thin gold wire connects between bonding pad and lead frame.
- **Encapsulation:** Lead frames are placed onto the mold plates and heated. Molten plastic material is pressed around each die to form its individual IC package.

- **Lead finish/trim and form:** Conductivity of the leads are improved by coating tin or lead solution. Then exact form of the leads as per package requirement is formed step by step.
- **Final testing and shipping:** Quality, reliabilty and functionality of the each chip is tested. Product type, date, package code etc are marked on to the IC packages. Individual chips are then put into antistatic tubes for shipping.

Source : http://asic-soc.blogspot.in/search/label/VLSI%20fabrication