OPERAND INSTRUCTIONS INVOLVING IMMEDIATE DATA

MOV
ADD/ADC/SUB/SBB \{ R/M, d8/d16
AND/OR/XOR/TEST/CMP

8 byte registers + 8 word registers + 24 byte memory + 24 word memory = 64 opcodes
10 instructions x 64 = 640 opcodes

3.3.1 Move Immediate data to a Register/ Memory location

Before                      After
MOV DX, ABCDH               DX 1234H    ABCDH

Before                      After
MOV BH, 12H                 BH 56H      12H

3.3.2 Add Immediate data to a Register/ Memory location

Before                      After
ADD [BX], 12H               BX 1000H

DS:1000H  20H              DS:1001H  32H
Before | After
---|---
ADD [BX], 1234H  |  BX 1000H
DS:1000H 2000H  |  3234H
DS:1002H

### 3.3.3 Add with Carry Immediate data to a Register/ Memory location

Before | After
---|---
ADC DH, 32H  |  DH 30H 63H
Add with Carry  |  Carry flag 1 0

63H= 0110 0011 It has four 1’s

New flag values: Ac=0, S=0, Z=0, V=0, P=1

### 3.3.4 Subtract Immediate data from a Register/ Memory location

Before | After
---|---
SUB DH, 40H  |  DH 30H F0H

Subtract (without borrow)

F0H=1111 0000 B(Four 1’s)

New flag values: Ac=0, S=1, Z=0, V=0, P=1, Cy=1

### 3.3.5 Subtract with borrow Immediate data from a Register/ Memory location
### 3.3.6 AND Immediate data with a Register/ Memory location

<table>
<thead>
<tr>
<th></th>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND BH, 0FH</td>
<td>BH 56H</td>
<td>06H</td>
</tr>
<tr>
<td></td>
<td>AND</td>
<td></td>
</tr>
</tbody>
</table>

56H = 0101 0110B

0FH = 0000 1111B

<table>
<thead>
<tr>
<th></th>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cy flag</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

06H = 0000 0110B(Two 1’s)

*Use*: Selectively reset to 0 some bits of the destination

- Bits that are ANDed with 0’s are reset to 0
- Bits that are ANDed with 1’s are not changed

### 3.3.7 OR Immediate data with a Register/ Memory location

<table>
<thead>
<tr>
<th></th>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR BH, 0FH</td>
<td>BH 56H</td>
<td>5FH</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
</tr>
</tbody>
</table>

56H = 0101 0110B
0FH = 0000 1111B
      CL 0FH

5FH = 0101 1111B

*Use:* Selectively set to 1 some bits of the destination

Bits that are ORed with 1’s are set to 1

Bits that are ORed with 0’s are not changed

### 3.3.8 Ex-OR Immediate data with a Register/ Memory location

<table>
<thead>
<tr>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR BH, 0FH</td>
<td>BH</td>
</tr>
<tr>
<td>56H = 0101 0110B</td>
<td>XOR</td>
</tr>
<tr>
<td>0FH = 0000 1111B</td>
<td>CL 0FH</td>
</tr>
<tr>
<td>59H = 0101 1001B</td>
<td></td>
</tr>
</tbody>
</table>

*Use:* Selectively complement some bits of the destn.

Bits that are XORed with 1’s are complemented

Bits that are XORed with 0’s are not changed

### 3.3.9 Test immediate data with a Register/ Memory location

<table>
<thead>
<tr>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEST BH, 0FH</td>
<td>BH 56H</td>
</tr>
<tr>
<td>56H=0101 0110B</td>
<td>AND</td>
</tr>
<tr>
<td>0FH=0000 1111B</td>
<td>Temp 45H</td>
</tr>
</tbody>
</table>

06H
06H=0000 0110B

TEST basically performs AND operation. Result of AND is not stored in destination. It is stored in Temp register. Temp is not accessible to programmer. There is no instruction like MOV Temp, 67H. Only flags are affected.

Source : http://elearningatria.files.wordpress.com/2013/10/cse-iv-microprocessors-10cs45-notes.pdf